TI Precision Labs 精密實驗室
ADC 和 OP AMPS 概述

Speaker: Andrew Wang

Agenda

- How Driver Non-linear Range Affecting ADC system
- How Driver Noise Affecting ADC system
- SAR ADC Driver RC Optimization
- How Driver Bandwidth Affecting ADC system
- How Voltage Reference Affecting ADC system

How Driver Non-linear Range Affecting ADC System

Speaker: Andrew Wang

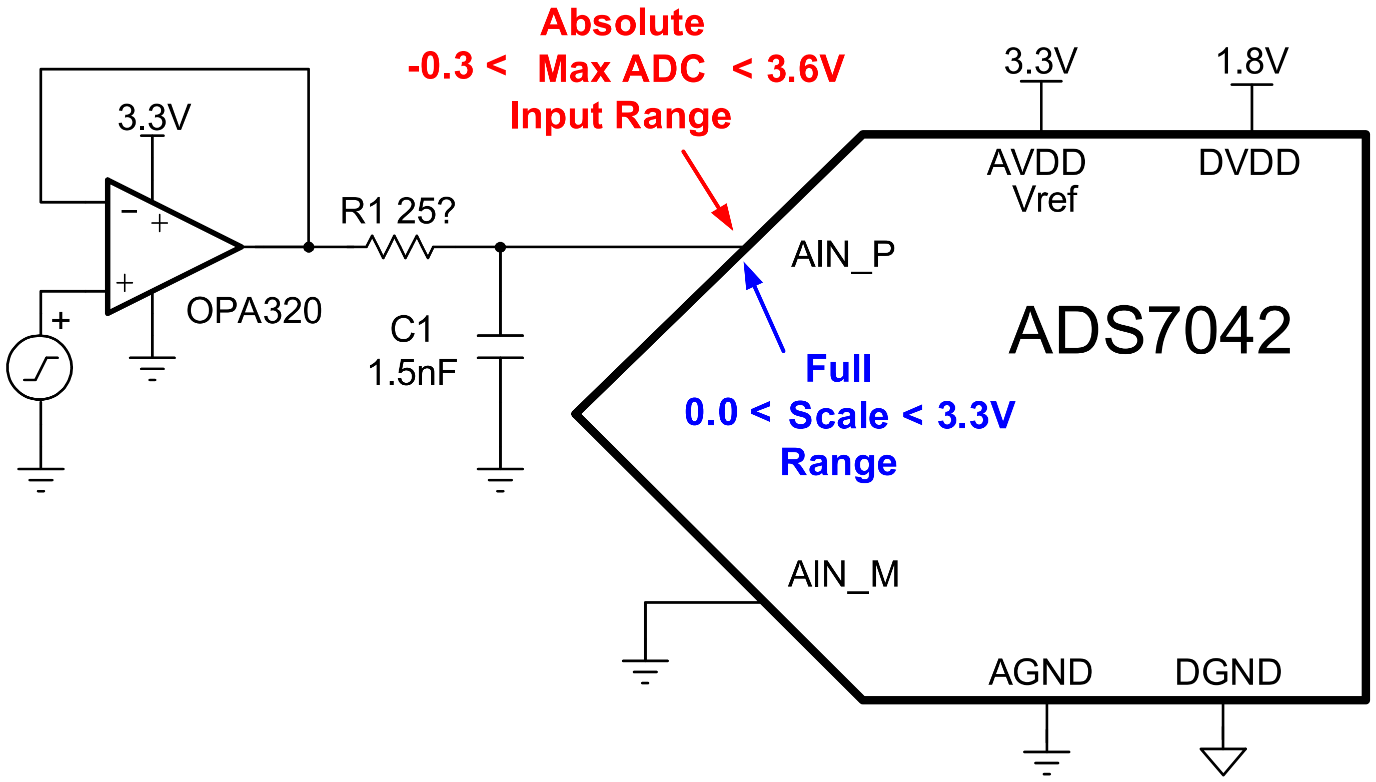
Single Ended Input: ADC Input Range Considerations

PARAMETER ADS7042		TEST CONDITION	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input voltage span			**0**		**AVDD**	V
Absolute Input voltage range	AINP to GND		0		AVDD+0.1	V
	AINM to GND		-0.1		+0.1	V

Absolute Maximum Ratings

ADS7042	MIN	MAX	UNIT
AVDD to GND	-0.3	3.9	V
DVDD to GND	-0.3	3.9	V
AINP to GND	**-0.3**	**AVDD + 0.3**	V
AINM to GND	-0.3	+0.3	V

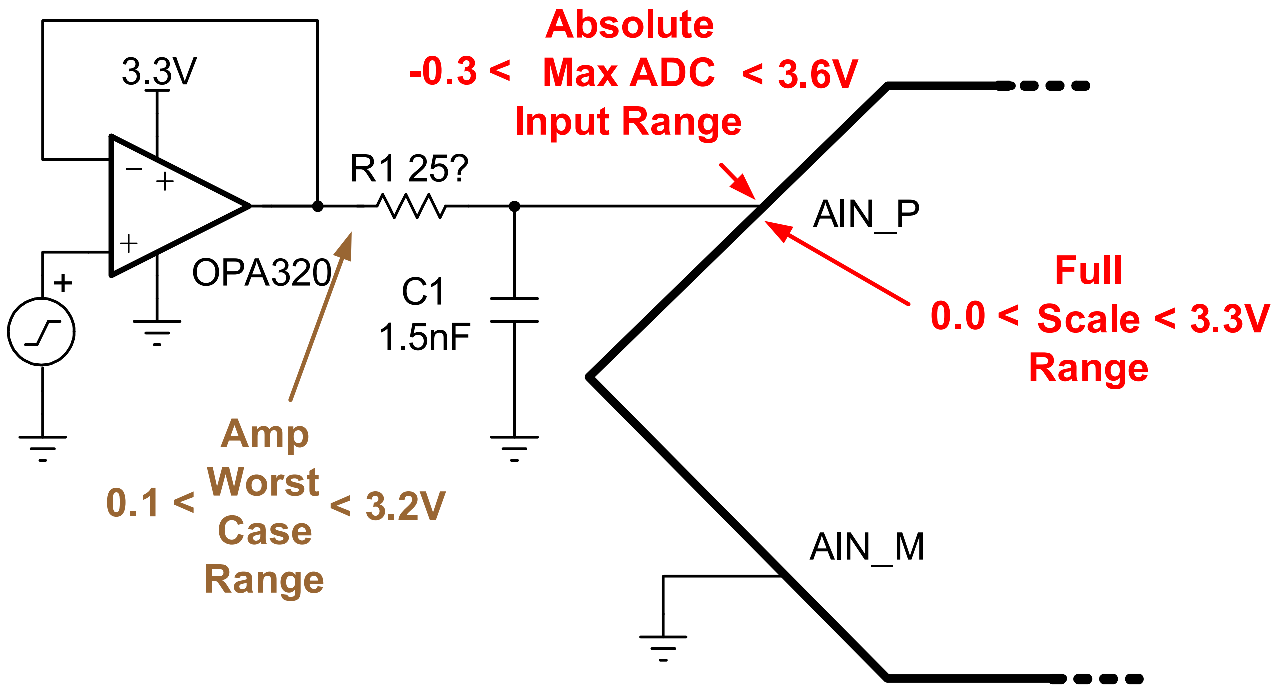
AVDD+0.3 = 3.3V + 0.3V = 3.6V



Single Ended Input: OPA320 Linear Range

PARAMETER OPA320		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
Common-mode voltage range	V_{cm}		(V-) - 0.1		(V+)+0.1	V
OUTPUT						
Voltage swing from both rails	V_O	RL = 10kΩ		10	20	mV
		RL = 2kΩ		25	35	
OPEN-LOOP GAIN						
Open-loop gain	A_{OL}	**0.1 < Vo < (V+)-0.1V, R_L = 10kΩ**	114	132		dB
		0.2 < Vo < (V+)-0.2V, R_L = 2kΩ	108	123		

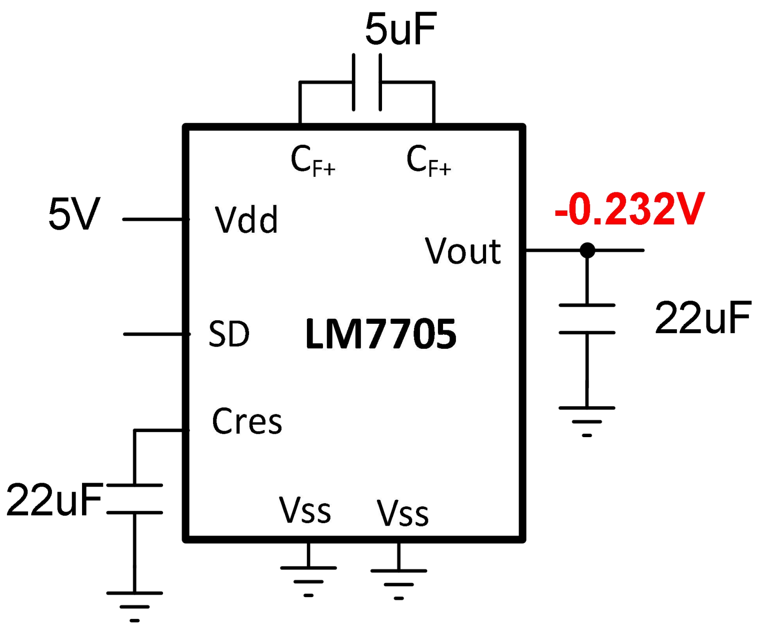
Amplifier Input Range	-0.1V < V_{cm} < 3.4V
Amplifier Output Range	0.02 < V_O < 3.28V
Amplifier Linear Range	0.1 < V_O < 3.2V
Worst Case Range	**0.1 < V_O < 3.2V**

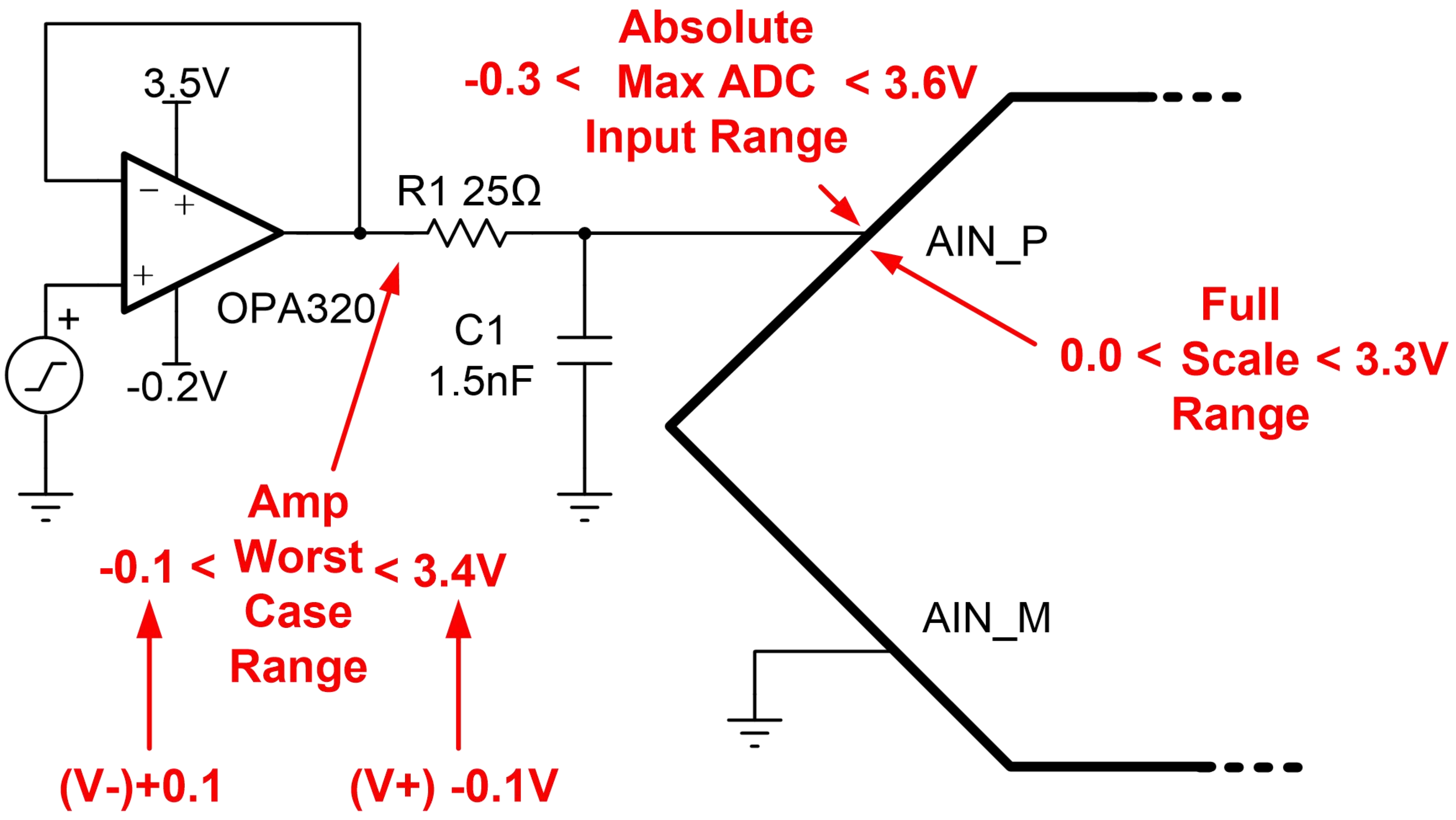


Single Ended Input: Extending the Op Amp Range

Low Noise Negative Bias Generator

- Regulated Output Voltage −0.232 V
- Output Voltage Tolerance 5%
- Output Voltage Ripple 4 mV_{PP}
- Maximum Output Current 26 mA

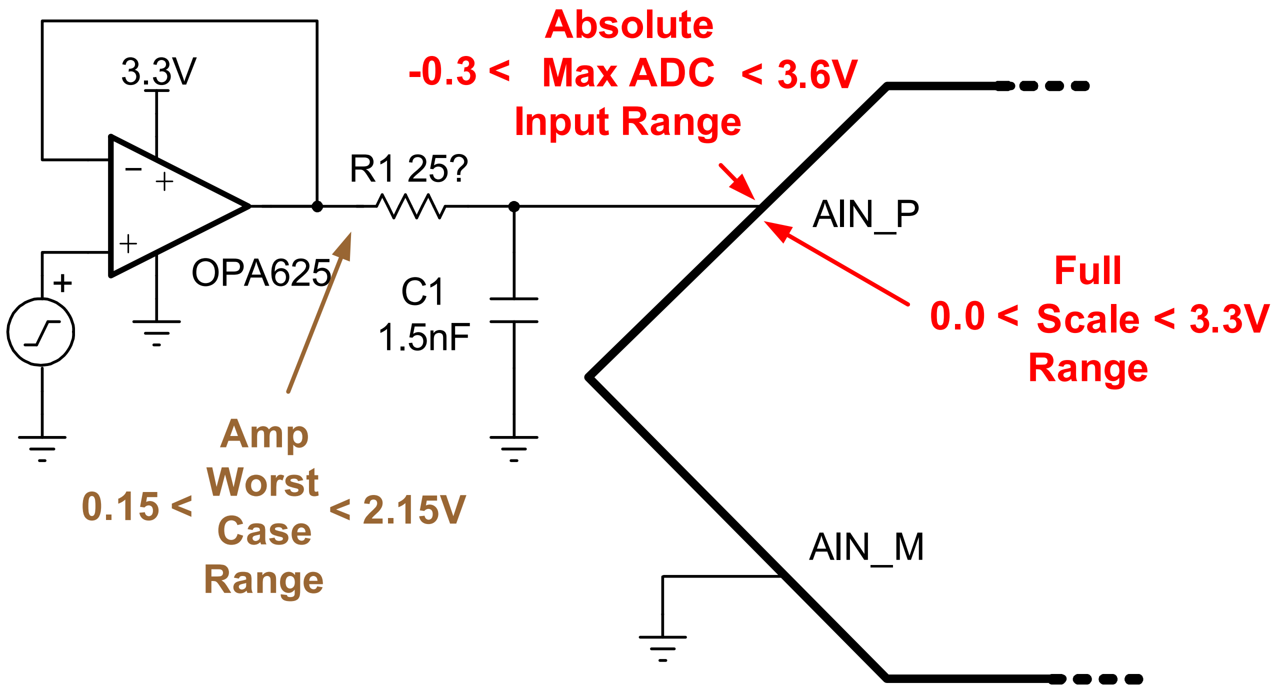




Single Ended Input: OPA625

PARAMETER OPA320		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
Common-mode voltage range	V_{cm}		(V-)		(V+) - 1.15	V
OUTPUT						
Voltage swing from both rails	V_O	RL = 10kΩ		20	35	mV
		RL = 600Ω		60	80	
OPEN-LOOP GAIN						
Open-loop gain	A_{OL}	0.15 < Vo < (V+) - 0.15V, R_L = 10kΩ	110	132		dB
		0.2 < Vo < (V+) - 0.2V, R_L = 600Ω	106	128		

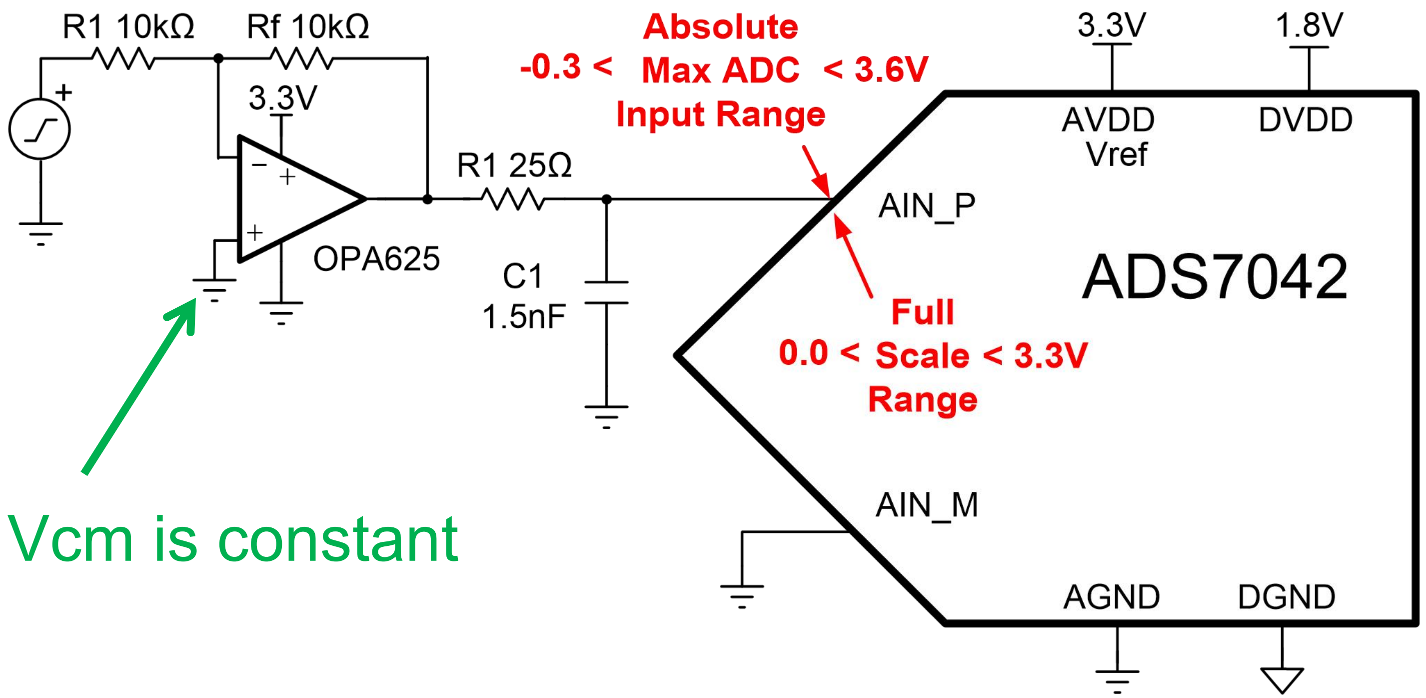
Amplifier input range	$0.0V < V_{cm} < 2.15V$
Amplifier output range	$0.035 < V_O < 3.265V$
Amplifier Linear Range	$0.15 < V_O < 3.15V$
Worst Case Range	$0.15 < V_O < 2.15V$



Inverting amplifier: Eliminate Common mode issue

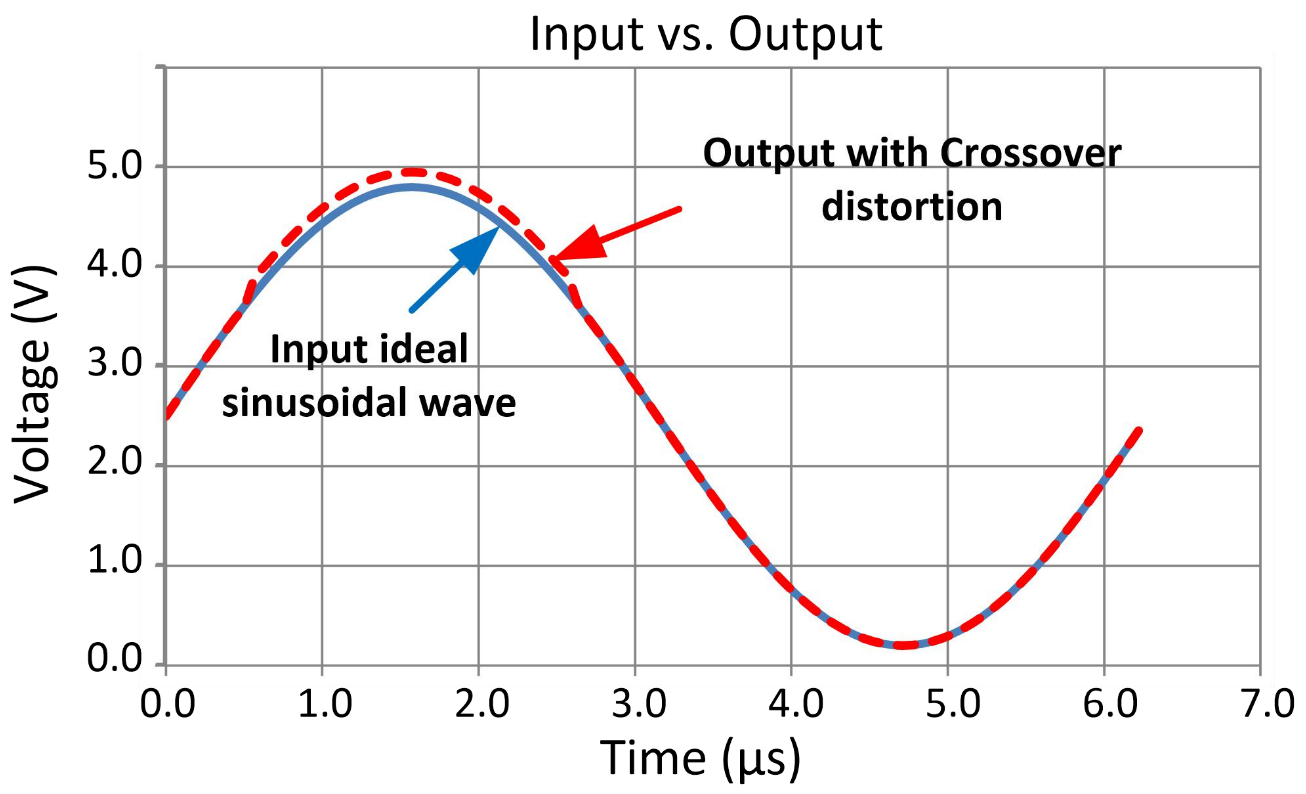
PARAMETER OPA625		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
Common-mode voltage range	V_{cm}		(V-)		(V+) - 1.15	V
OUTPUT						
Voltage swing from both rails	V_O	RL = 10kΩ		20	35	mV
		RL = 600Ω		60	80	
OPEN-LOOP GAIN						
Open-loop gain	A_{OL}	0.15 < Vo < (V+) - 0.15V, R_L = 10kΩ	110	132		dB
		0.2 < Vo < (V+) - 0.2V, R_L = 600Ω	106	128		

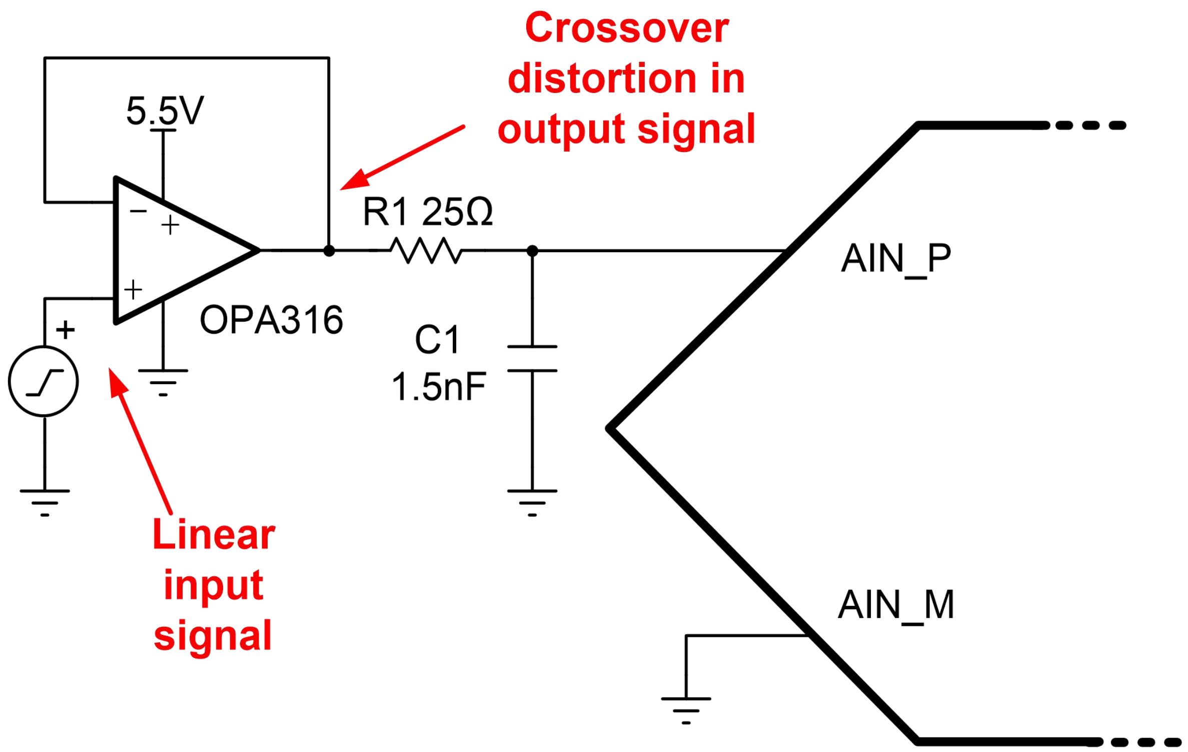
Amplifier input range	No Vcm limit
Amplifier output range	$0.035 < V_O < 3.265V$
Amplifier Linear Range	$0.15 < V_O < 3.15V$
Worst Case Range	**$0.15 < V_O < 3.15V$**



Input Crossover Distortion in Rail-to-Rail Inputs

PARAMETER OPA316		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE						
V_{CM}	Common mode voltage range	TA = -40C to 85C	-0.2		(V+)+0.1	V
CMRR	Common mode Rejection	Vs = 5V, -0.1V<Vcm< 3.6V	76	90		dB
		Vs = 5V, -0.1V<Vcm<5.2V	65	80		dB

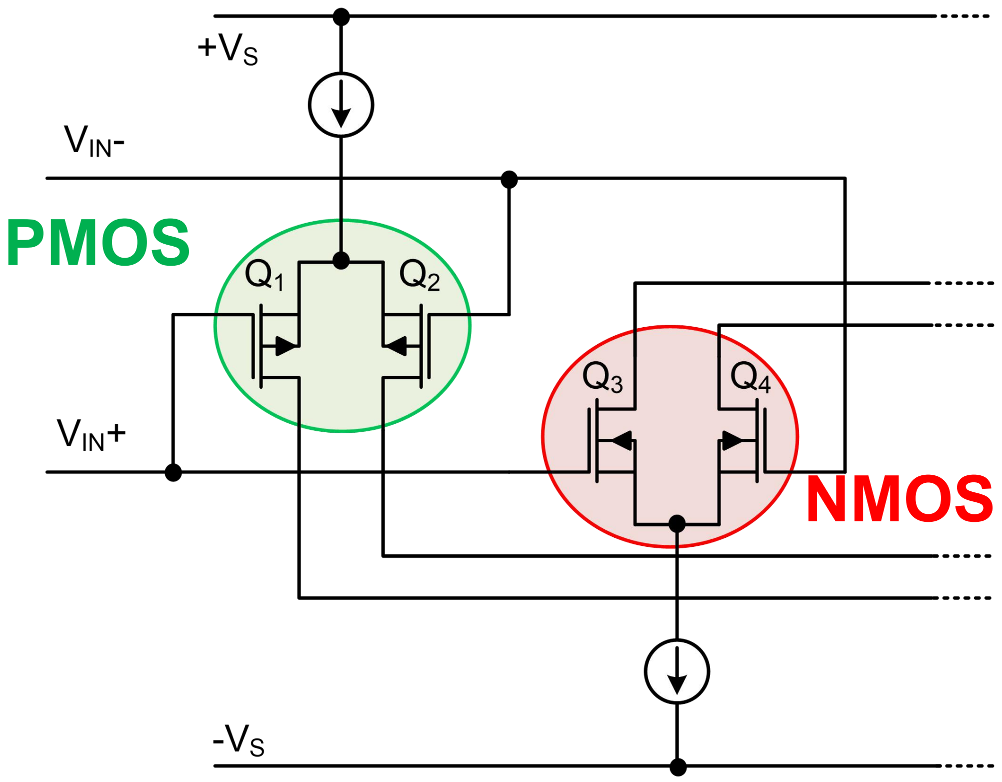


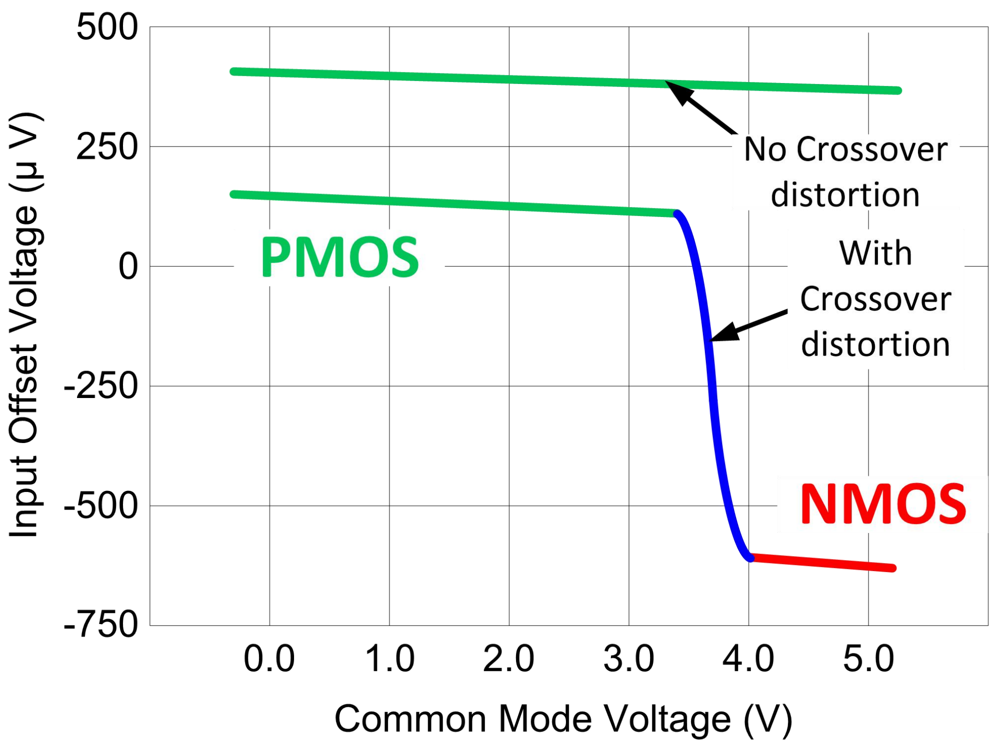


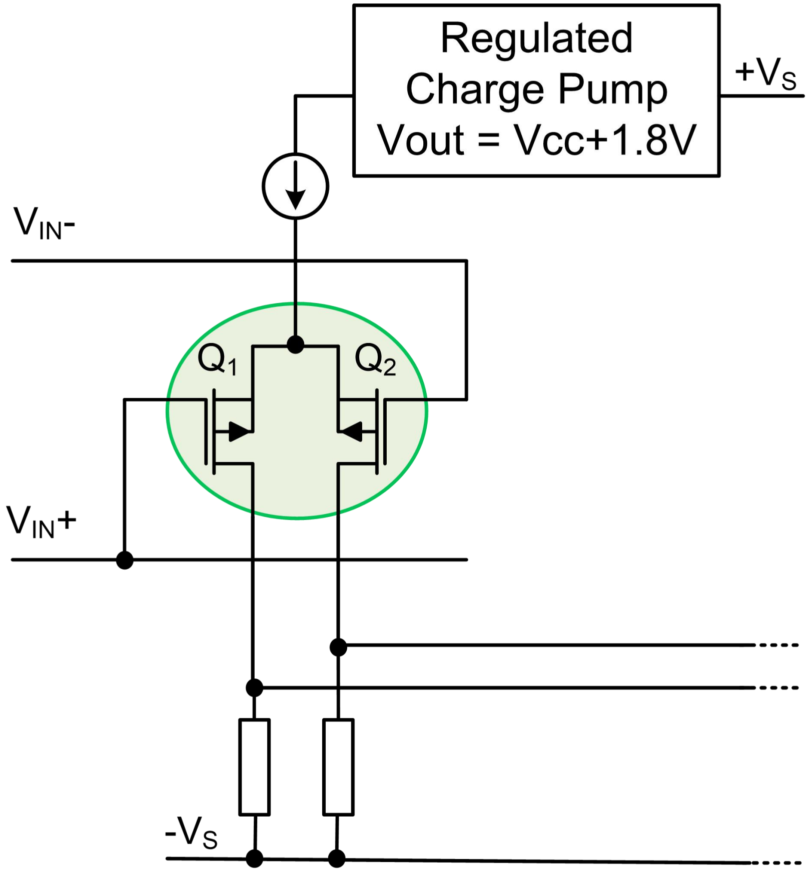
Input Cross-Over distortion vs Zero Cross-Over

PARAMETER: OPA350 – Has Crossover		MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE					
V_{CM}	Common mode voltage range	(V-)-0.1		(V+)+0.1	V
CMRR	Common mode Rejection -0.1V<Vcm<5.6V	74	90		dB

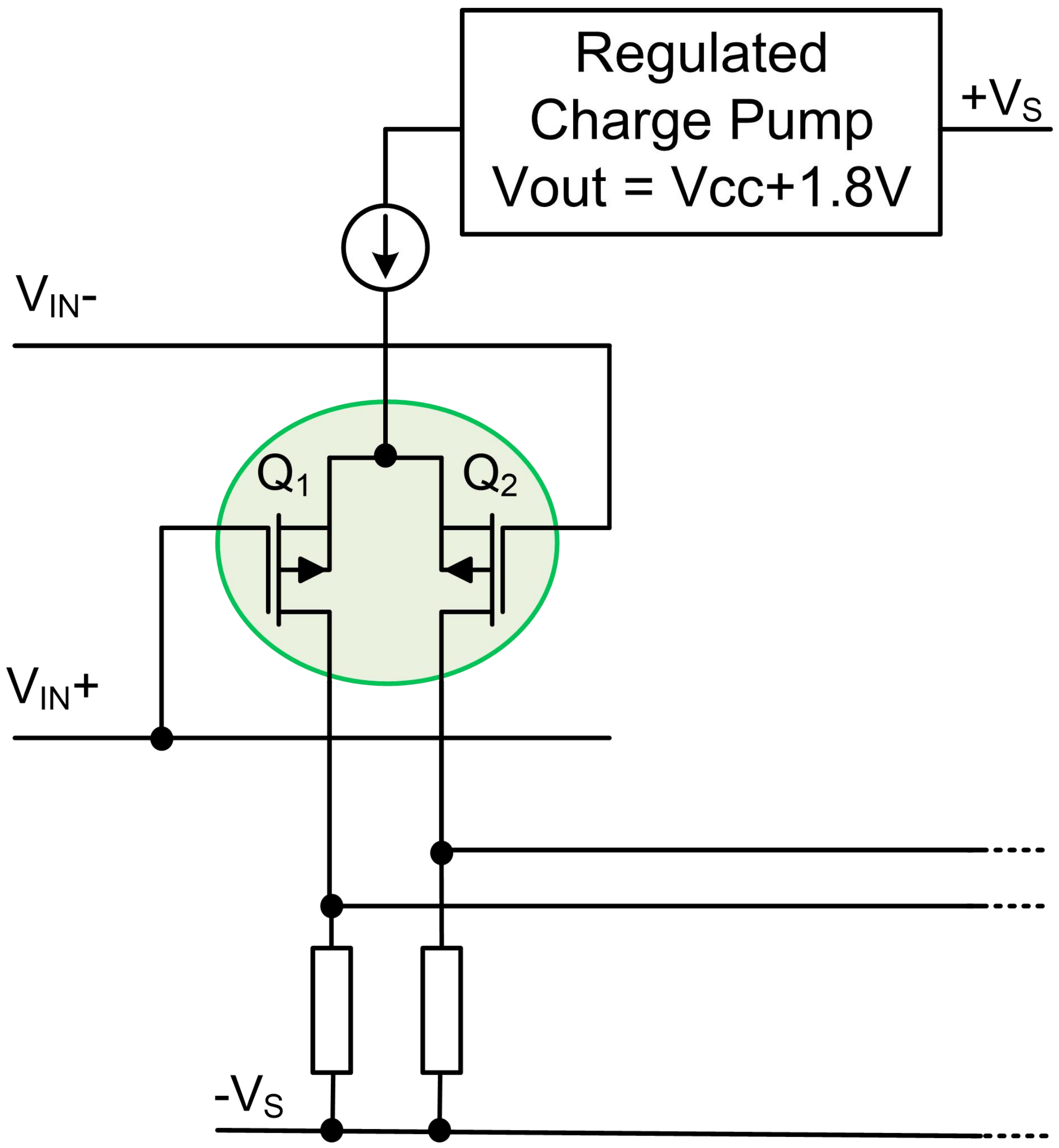
PARAMETER: OPA320 – Zero Cross-Over		MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE					
V_{CM}	Common mode voltage range	(V-)-0.1		(V+)+0.1	V
CMRR	Common mode Rejection -0.1V<Vcm<5.6V	100	114		dB



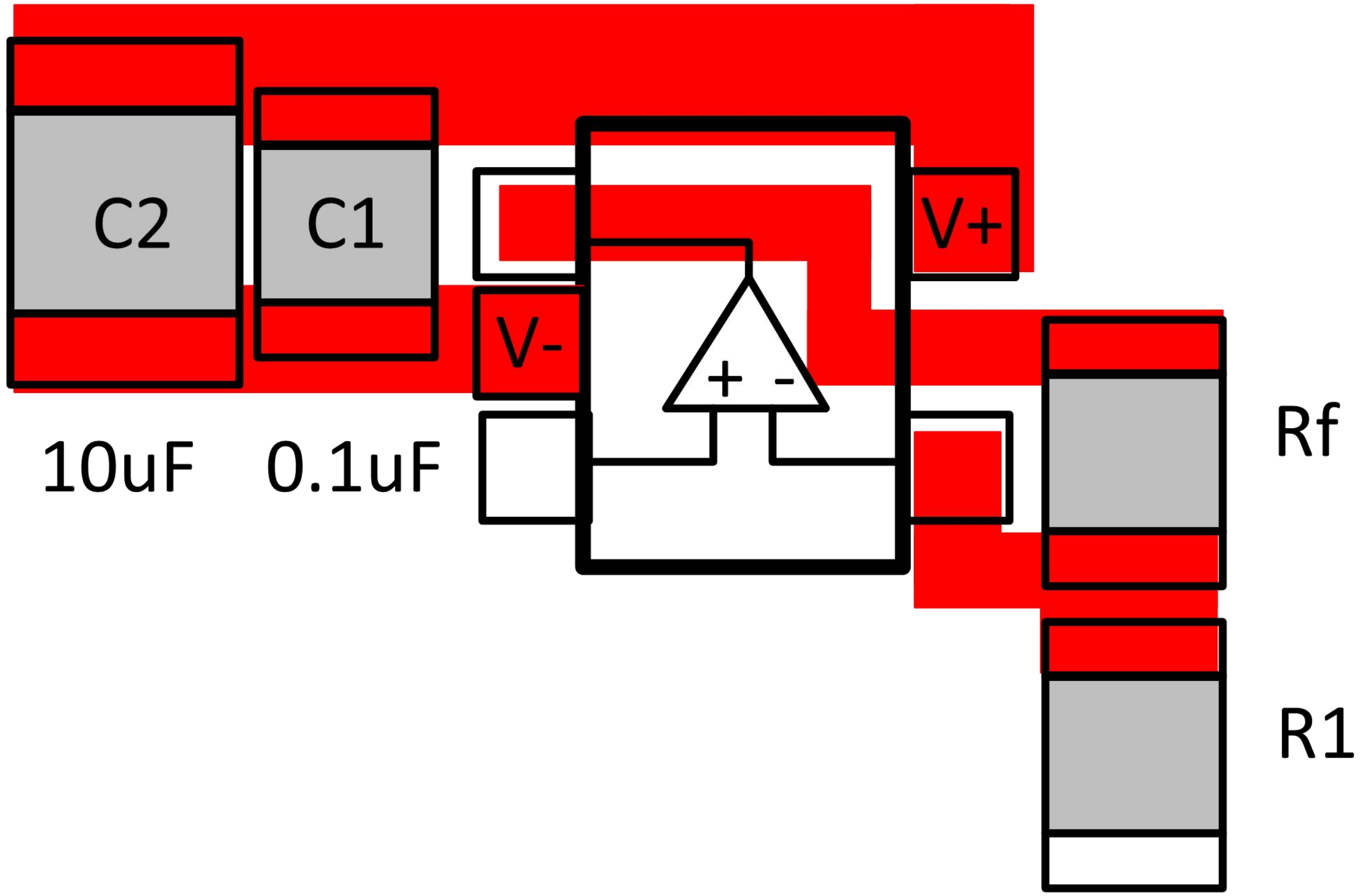




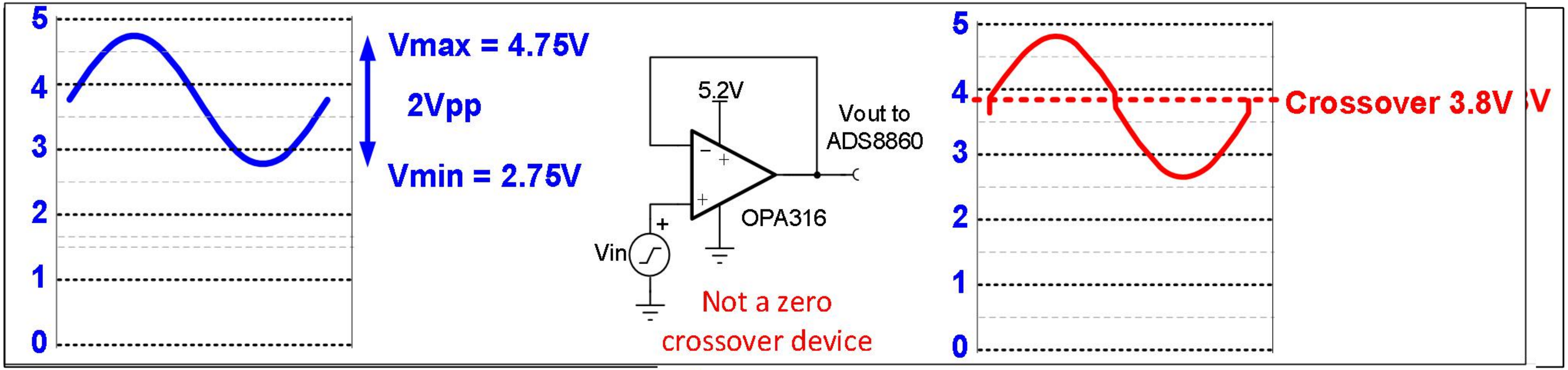
Optimize bypass for internal charge pump op amps

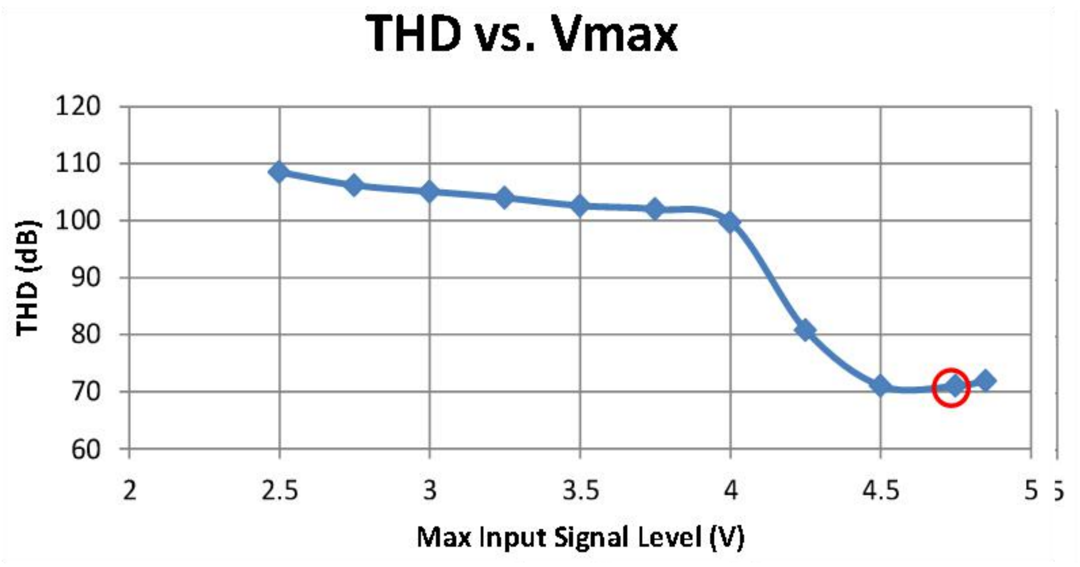


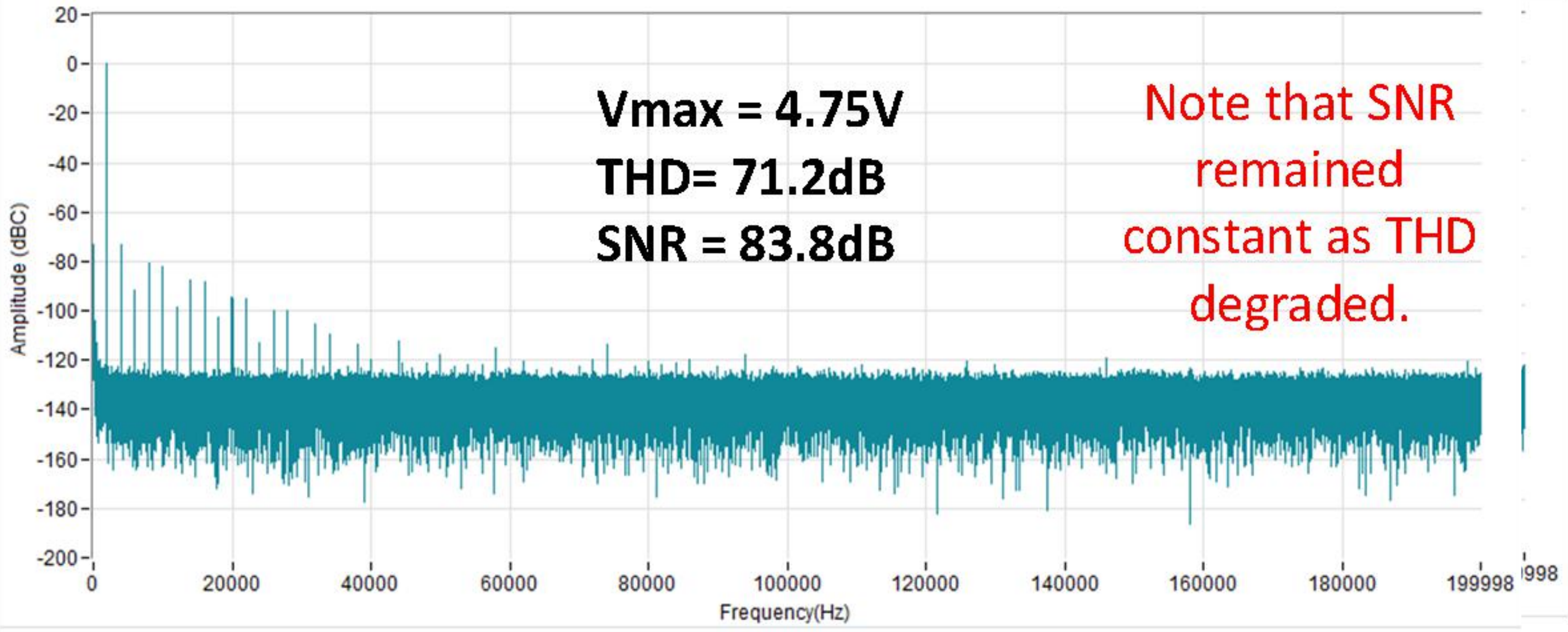
Short direct connections from supply to decoupling



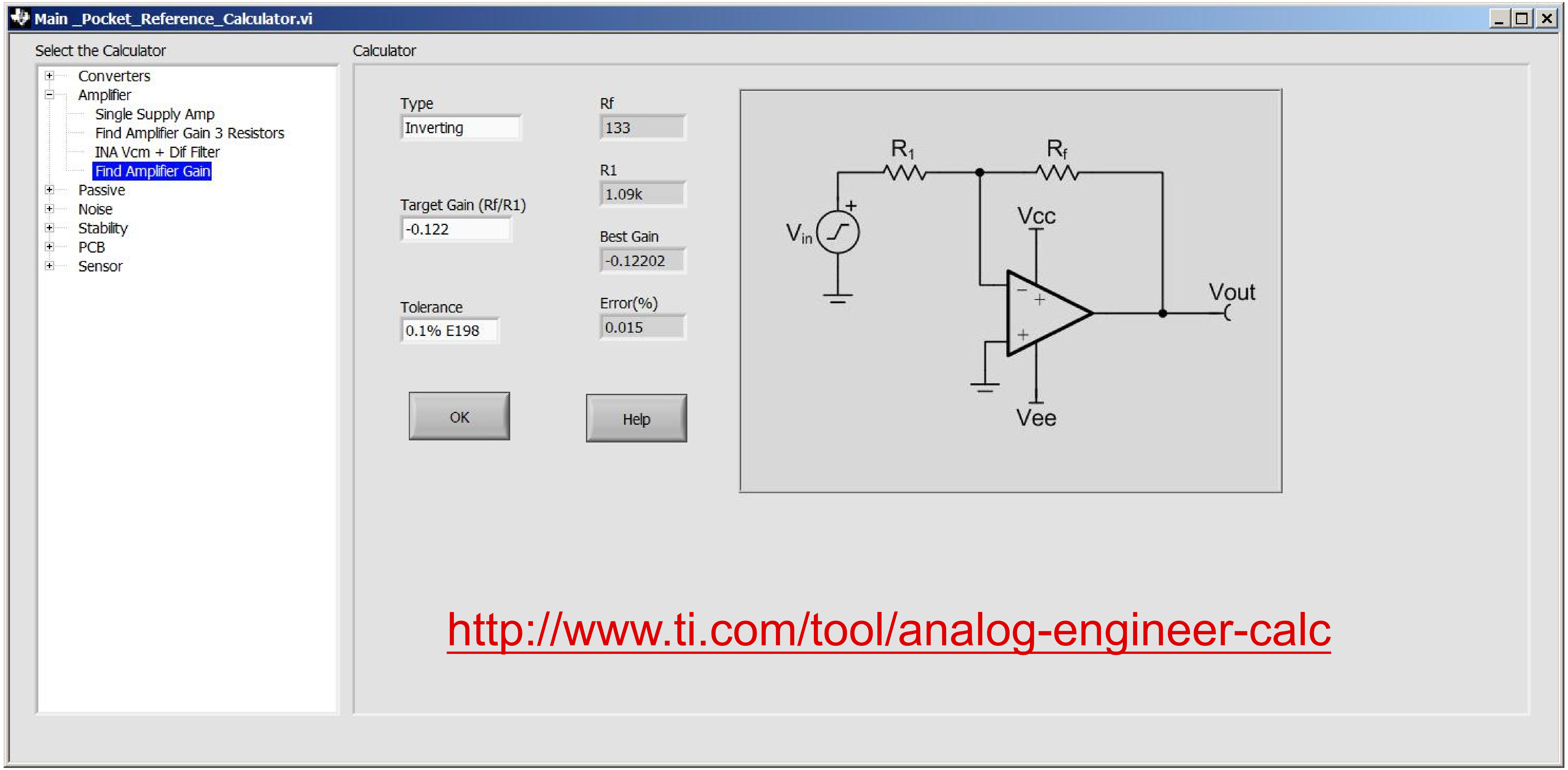
THD vs. Input Crossover Distortion







Finding standard resistors for unusual gains

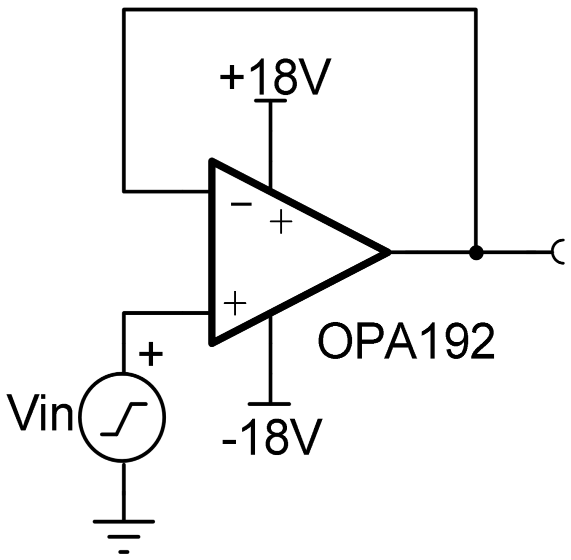


http://www.ti.com/tool/analog-engineer-calc

quick quiz.

Quiz: Linear Range ADC + OPA

4. The amplifier shown below ______.
   a. Would have poor power supply rejection.
   b. Would show crossover distortion if the input signal is greater than 15Vpk.
   c. Would not show crossover distortion.
   d. Would have a low input impedance.



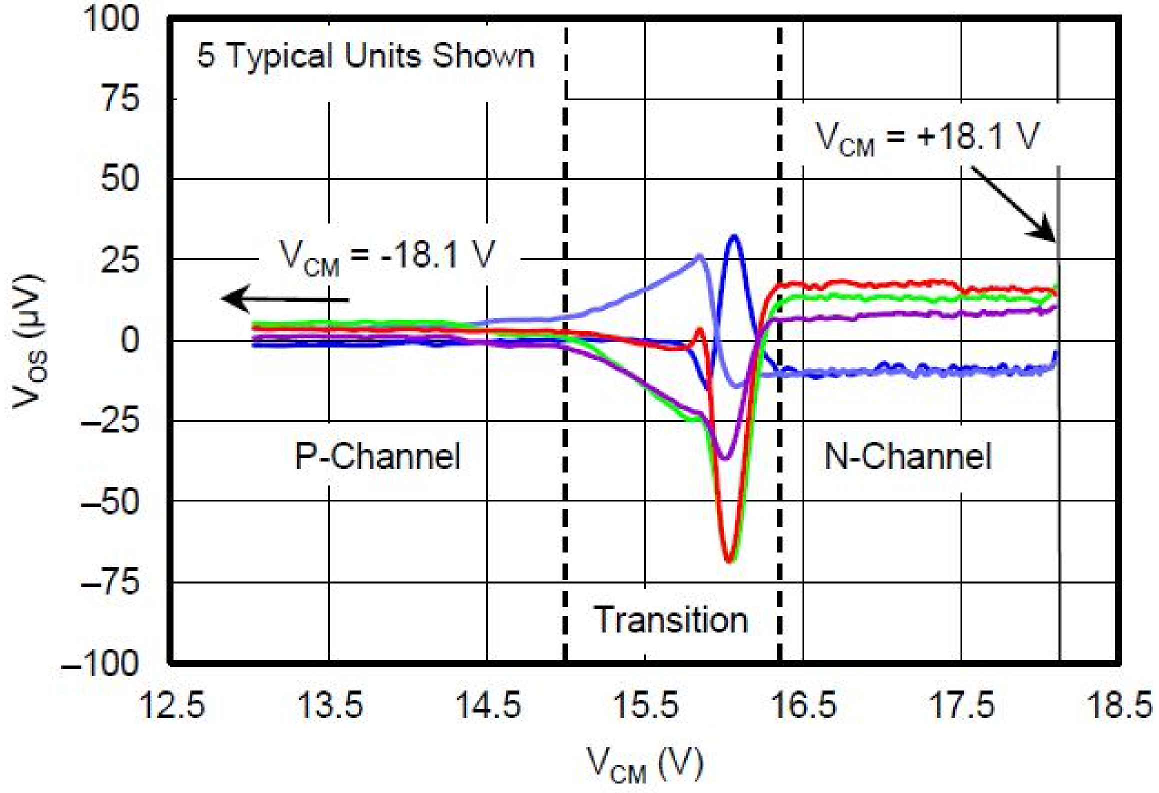
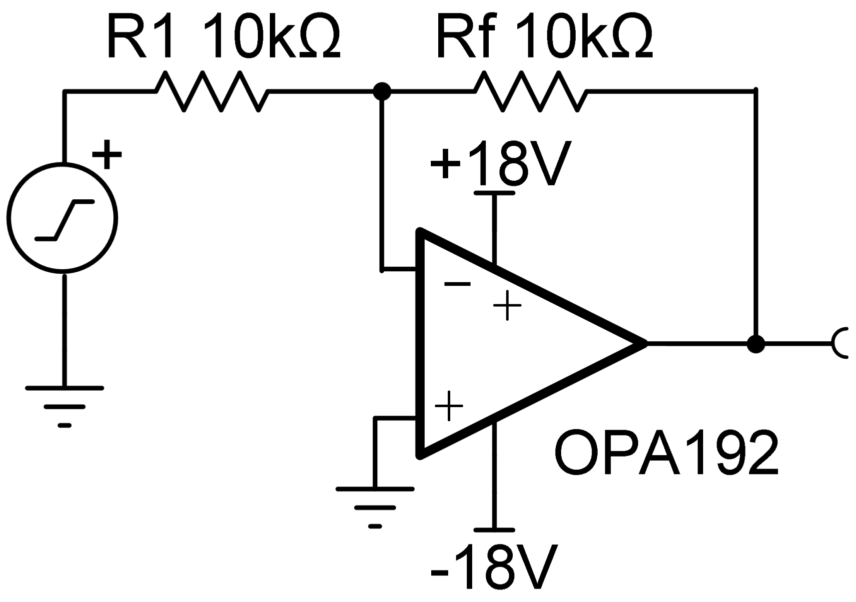


Figure 13: Offset Voltage vs. Common-Mode Voltage

Quiz: Linear Range ADC + OPA

5. The amplifier shown below ______.
   a. Would have poor power supply rejection.
   b. Would show crossover distortion if the input signal is greater than 15Vpk.
   c. Would not show crossover distortion.
   d. Would have a high input impedance.



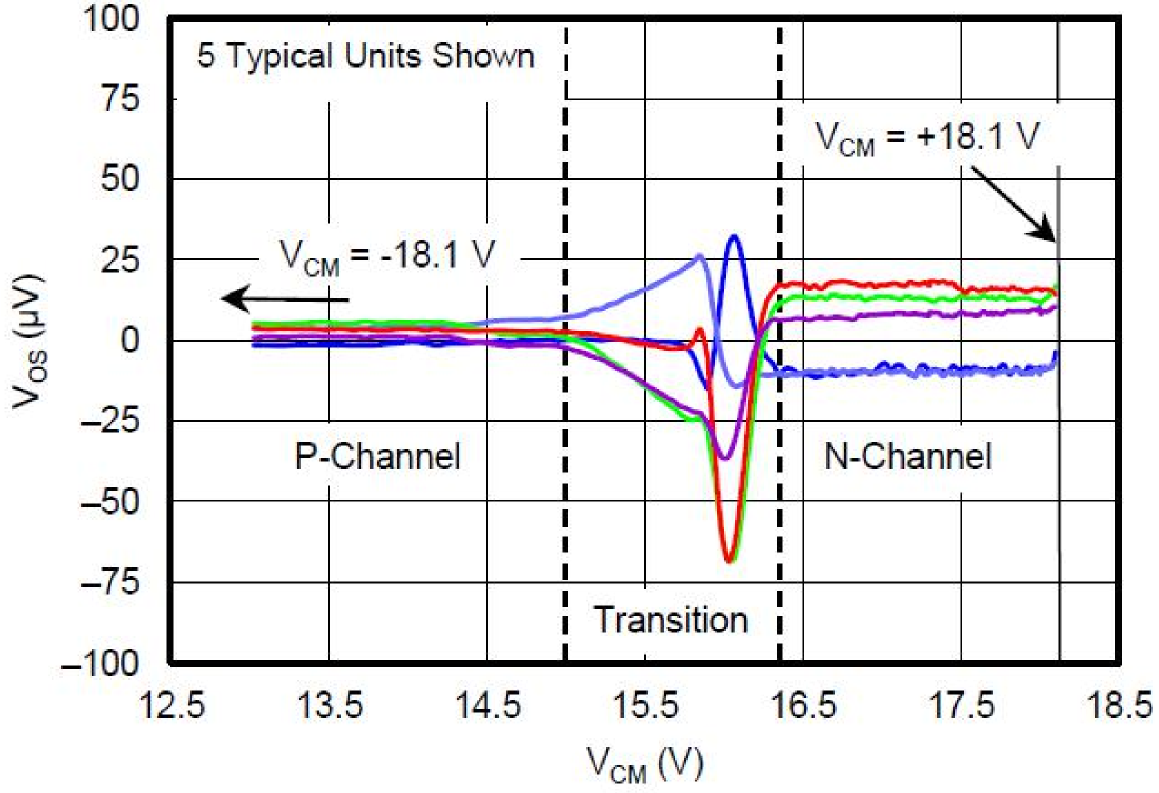
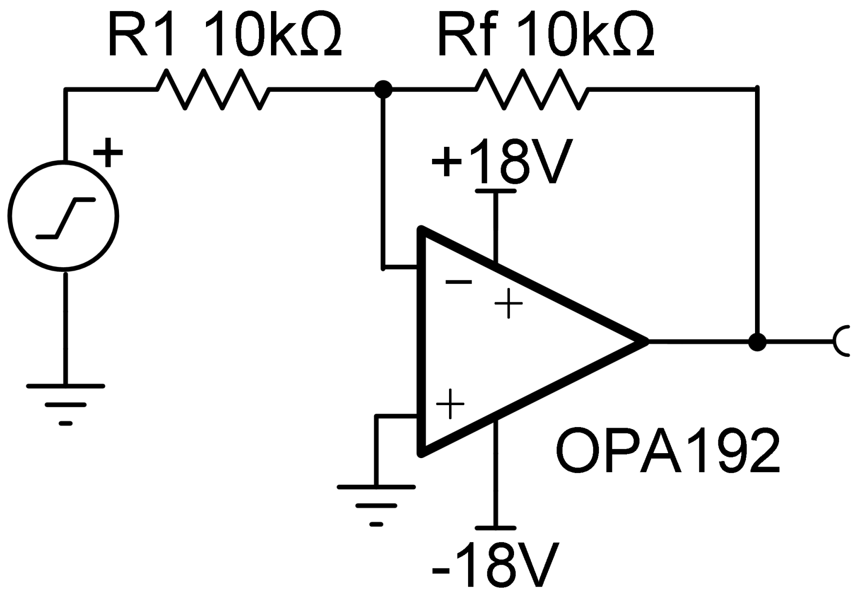


Figure 13: Offset Voltage vs. Common-Mode Voltage

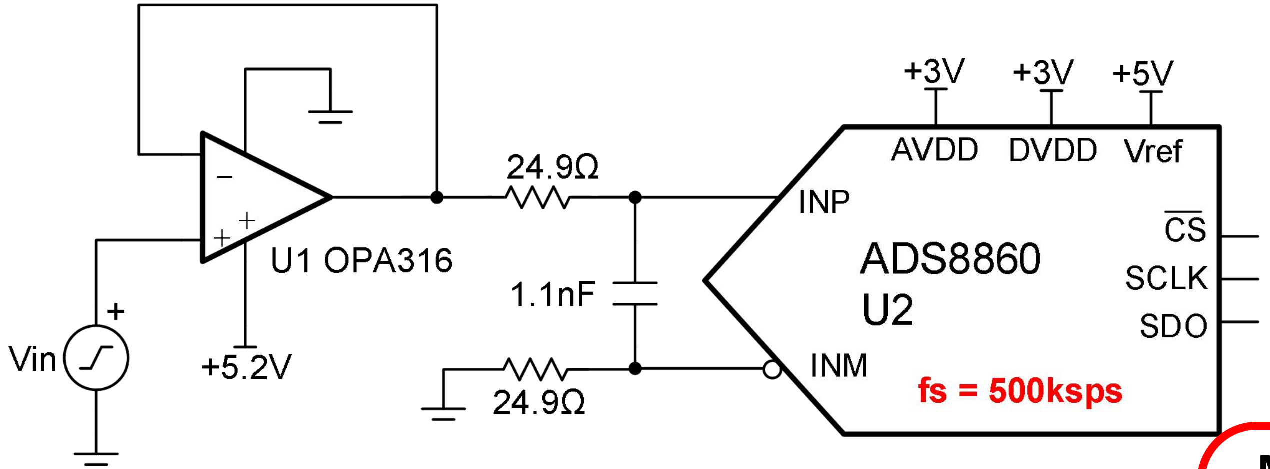
Quiz: Linear Range ADC + OPA

6. Which of the following applies to an inverting amplifier topology.
    a. Gain error is determined by resistor tolerance.
    b. The input impedance is relatively low (10kΩ in this case).
    c. The circuit will not have crossover distortion issues.
    d. The output will be loaded by the feedback network (10kΩ in this case).
    e. All the statements apply to the inverting topology.
    f. None of the statements apply to the inverting topology.



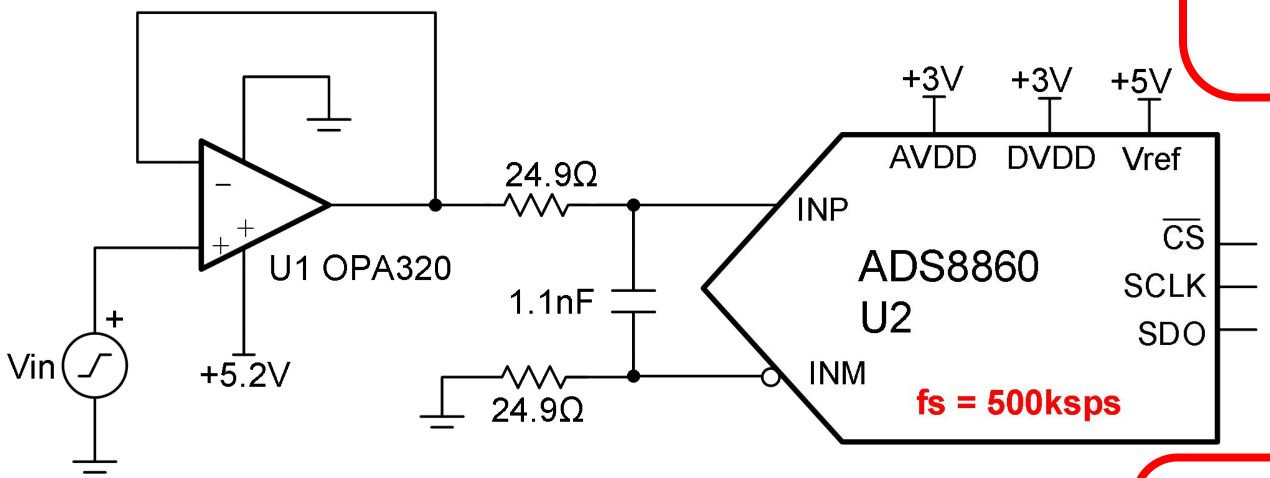
Crossover Distortion
Experiment

Op Amp with and without input Crossover distortion



PARAMETER: OPA316 – Has Crossover		MIN	TYP	MAX	UNIT
V_{CM}	Common Mode Voltage	(V-)-0.2		(V+)+0.2	V
CMRR	(V-)-0.2 < Vcm < (V+)-1.4V	76	90		dB
	(V-)-0.2 < Vcm < (V+)+0.2V	65	80		

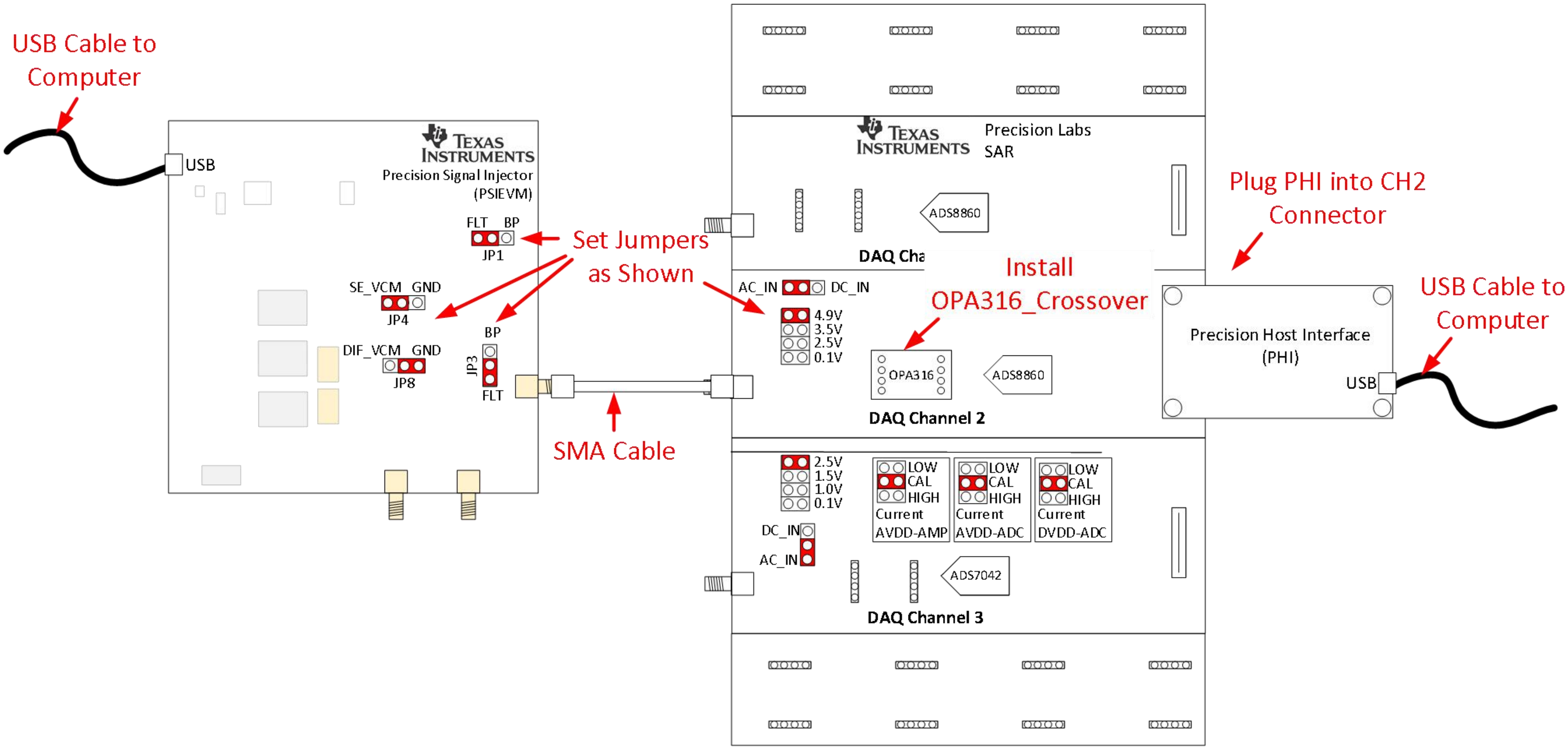
Much better CMRR 1.4V below positive rail. For 5.2V supply, crossover happens at 3.8V (5.2V – 1.4V = 3.8V)



PARAMETER: OPA320 – No Crossover		MIN	TYP	MAX	UNIT
V_{CM}	Common Mode Voltage	(V-)-0.1		(V+)+0.1	V
CMRR	(V-)-0.1 < Vcm < (V+)+0.1V	100	114		dB

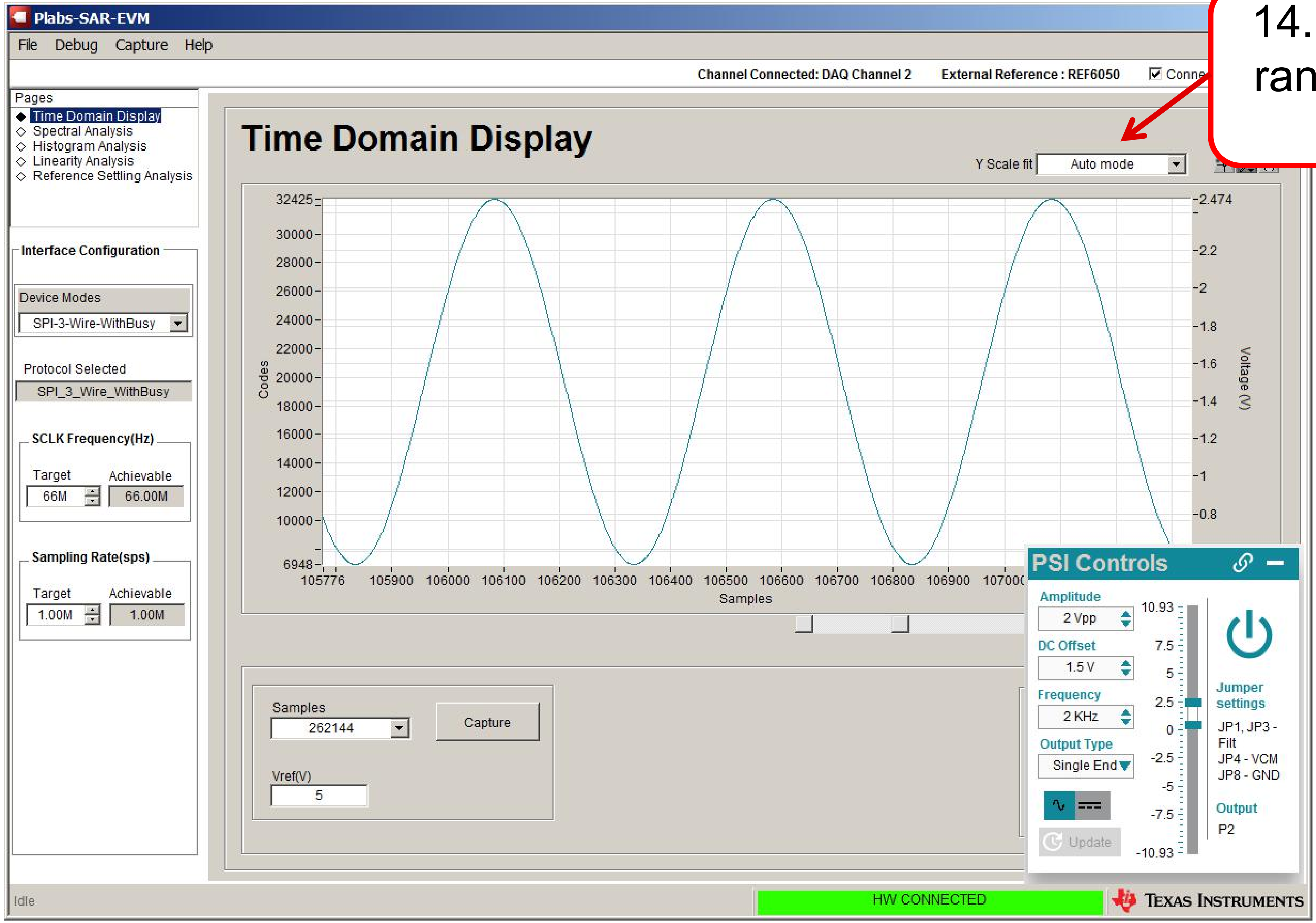
Much better CMRR across entire common mode range.

1a: Connect the hardware



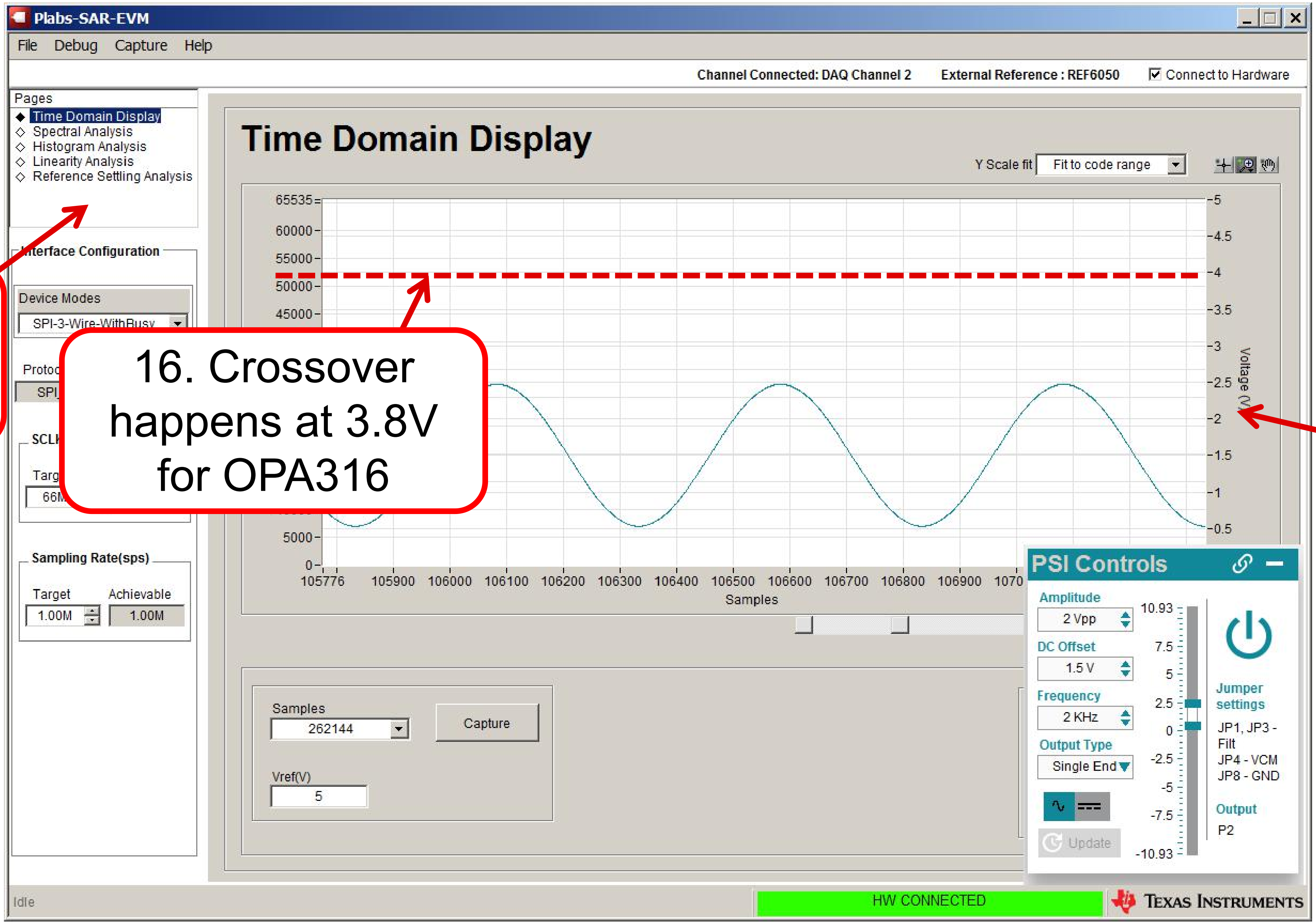
Demo – Driver Crossover

Capture the waveform and zoom in.



14. Select “Fit Code to range” to show the full scale range.

Capture the waveform and zoom in.

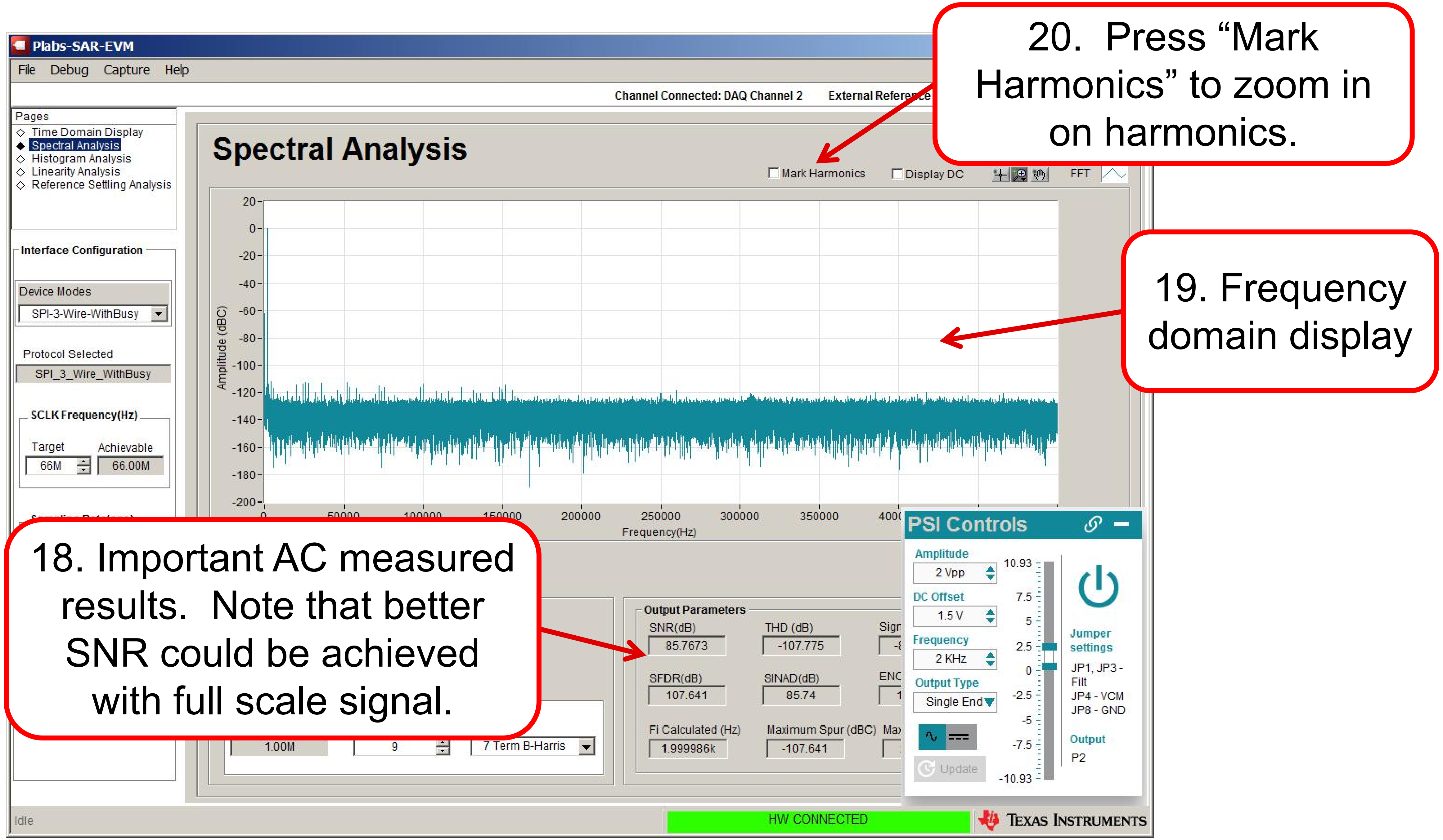


17. Change to "Spectral Analysis"

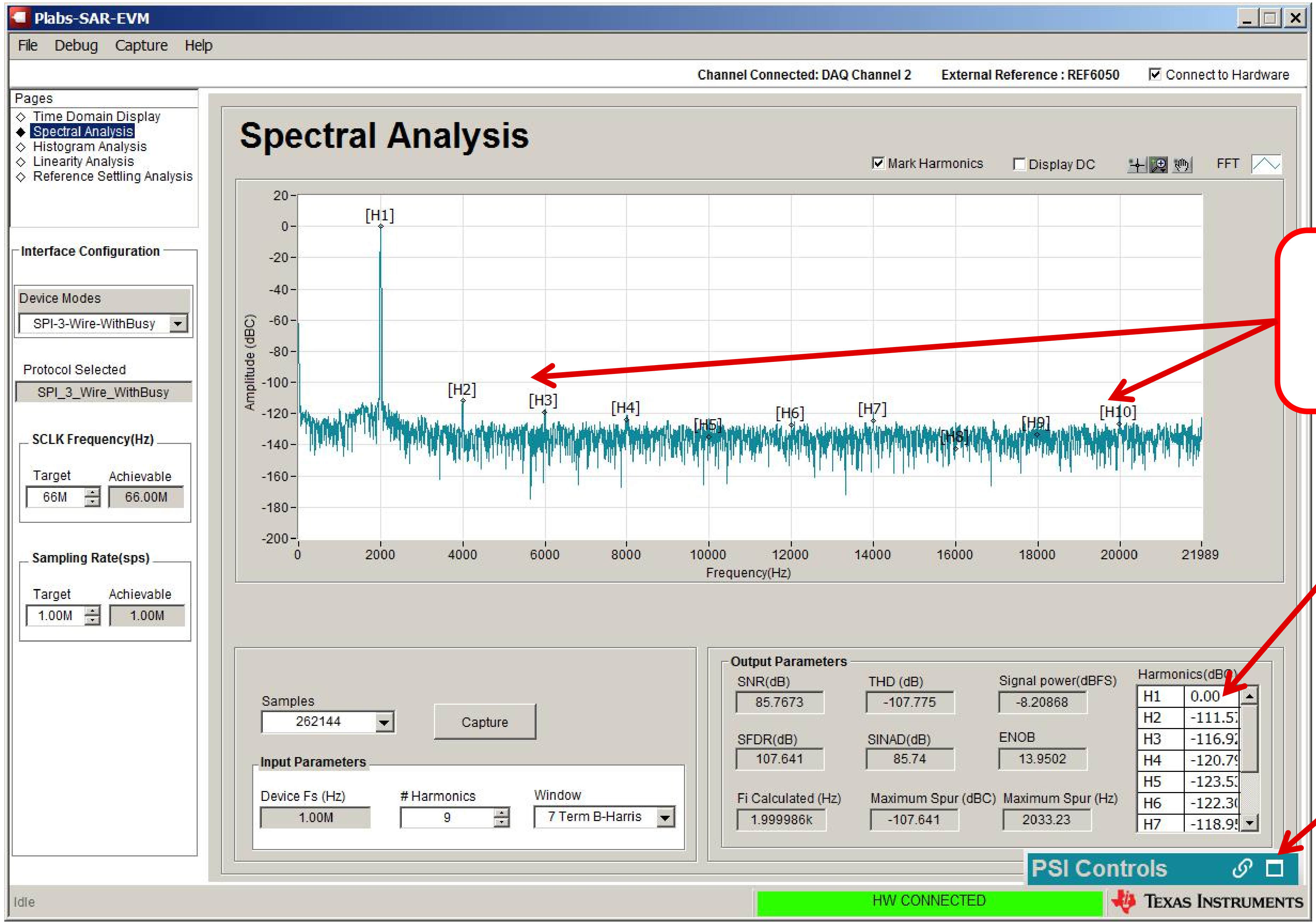
16. Crossover happens at 3.8V for OPA316

15. Now you can see that the full scale range is displayed (5V) in this example.

Frequency Domain Results



Mark Harmonics



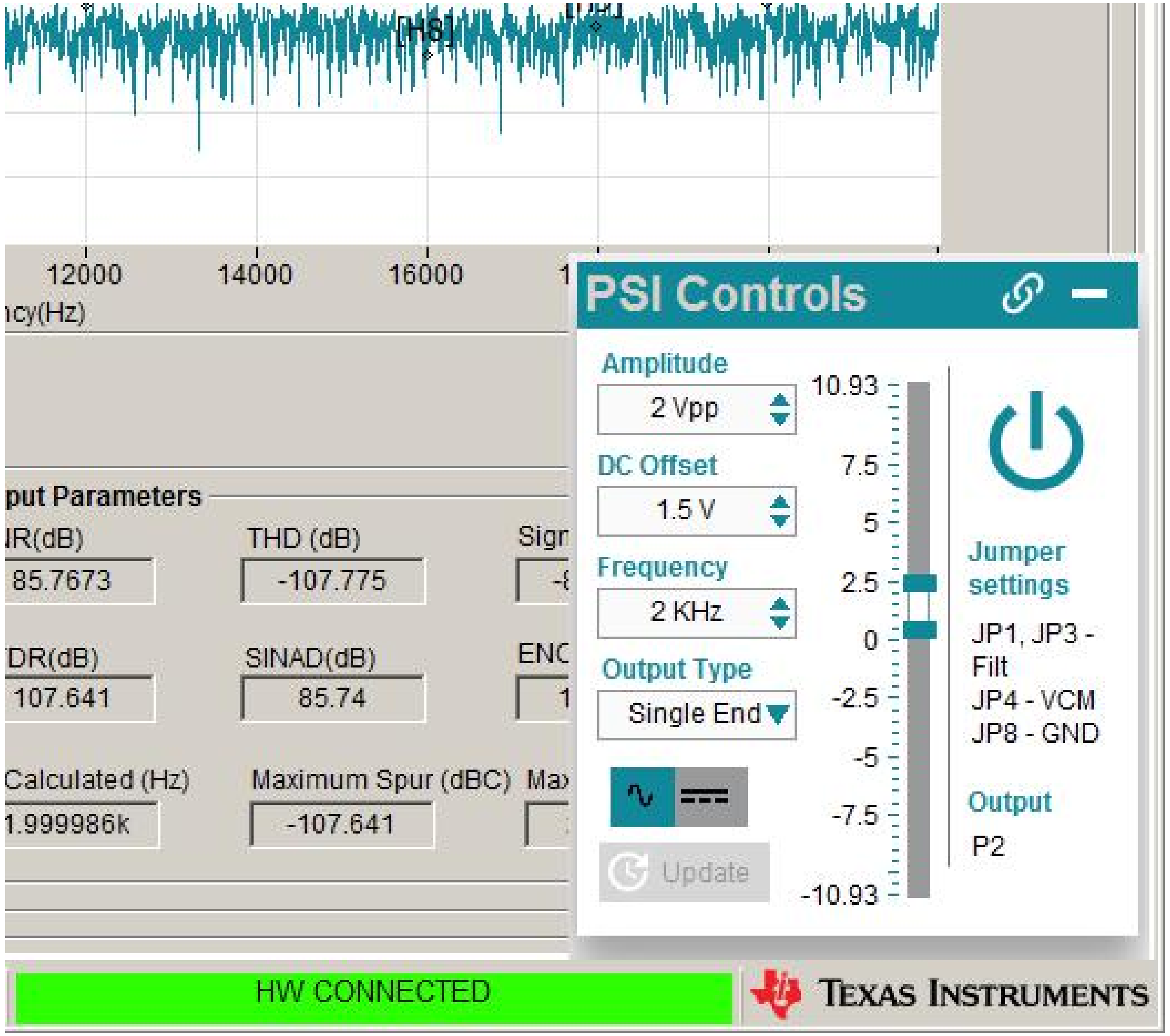
21. Zoom in on harmonics marked H2 …H10

22. Amplitude of harmonics in table form.

23. Minimize or maximize PSI controls as needed.

Enter Vin, Vcm to compare OPA316 and OPA320

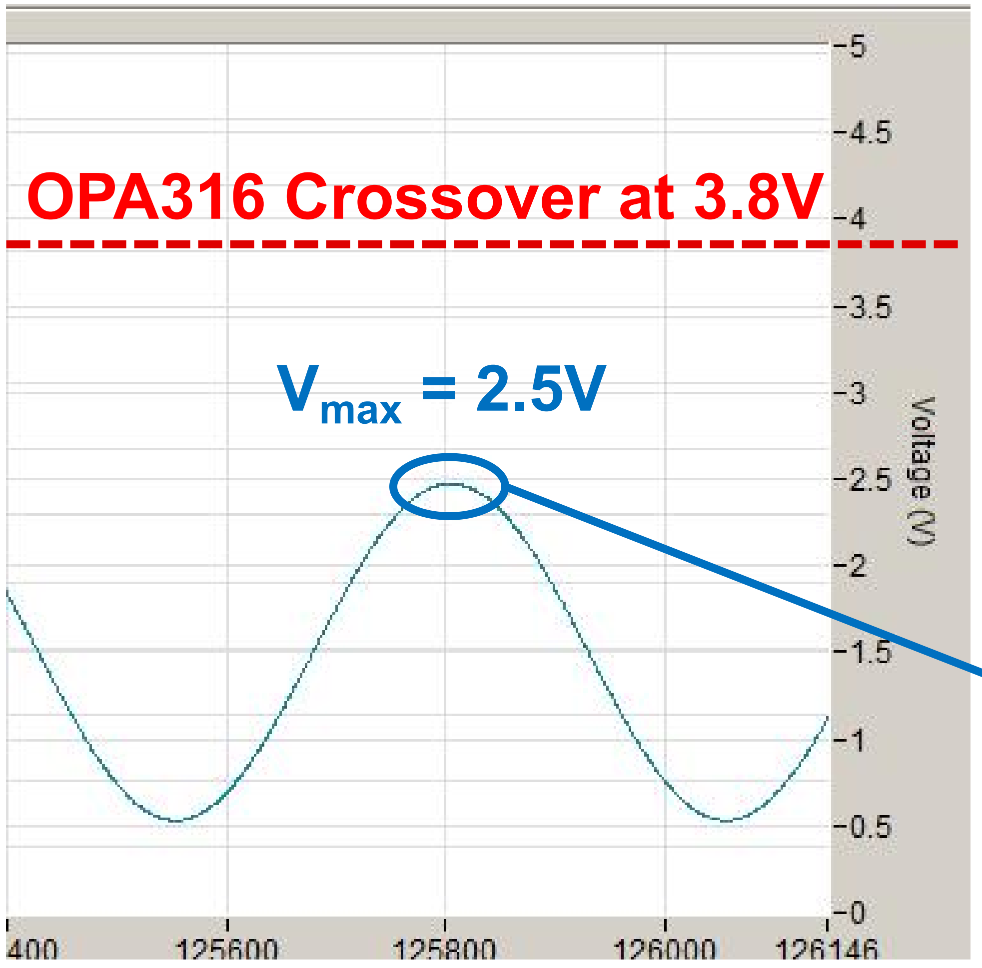
fin = 2kHz, fsamp = 500kHz Crossover region at 3.8V on OPA316					
PSI Signal Settings		**Calculated PSI Min and Max Output**		**OPA316 Expected**	
Vin (Vpp)	Vcm (V)	Vmin (V)	Vmax (V)	SNR (dB)	THD (dB)
2	1.5	0.5	2.5	85.3	-104.4
2	2	1	3	85.3	-102.9
2	3	2	4	85.2	-98.8
2	3.2	2.2	4.2	85.2	-83.8
2	3.5	2.5	4.5	85.1	-76.1
2	3.8	2.8	4.8	85.0	-77.2

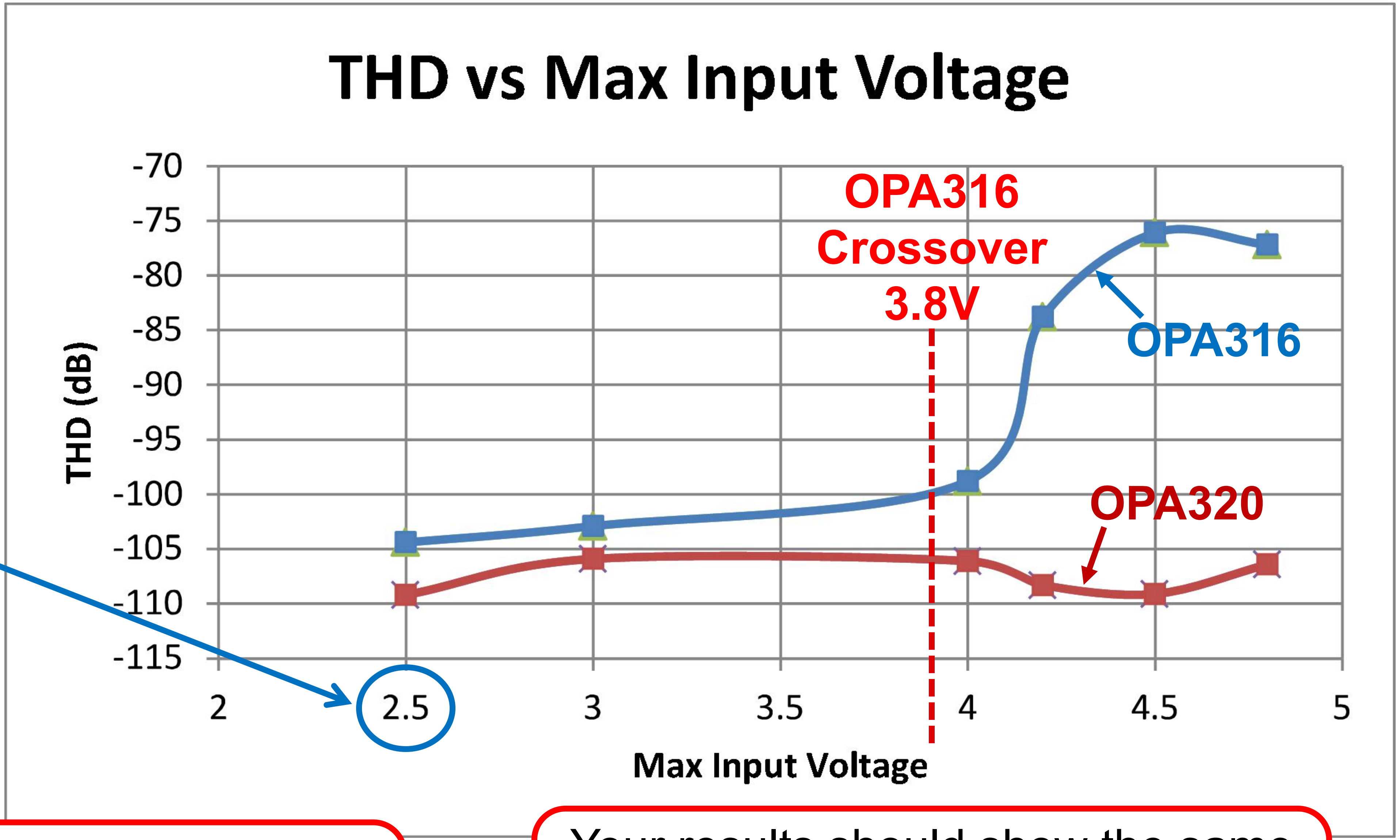


1b:Measured vs Expected Results

fin = 2kHz, fsamp = 500kHz Crossover region at 3.8V on OPA316							
PSI Signal Settings		**Calculated PSI Min and Max Output**		**OPA316 Crossover Expected**		**OPA320 Goodfilter1 Expected**	
Vin (Vpp)	Vcm (V)	Vmin (V)	Vmax (V)	SNR (dB)	THD (dB)	SNR (dB)	THD (dB)
2	1.5	0.5	2.5	85.3	-104.4	85.7	-109.2
2	2	1	3	85.3	-102.9	85.6	-105.9
2	3	2	4	85.2	-98.8	85.7	-106.1
2	3.2	2.2	4.2	85.2	-83.8	85.6	-108.3
2	3.5	2.5	4.5	85.1	-76.1	85.6	-109.1
2	3.8	2.8	4.8	85.0	-77.2	85.7	-106.4

Graph of results





Microsoft Excel Worksheet

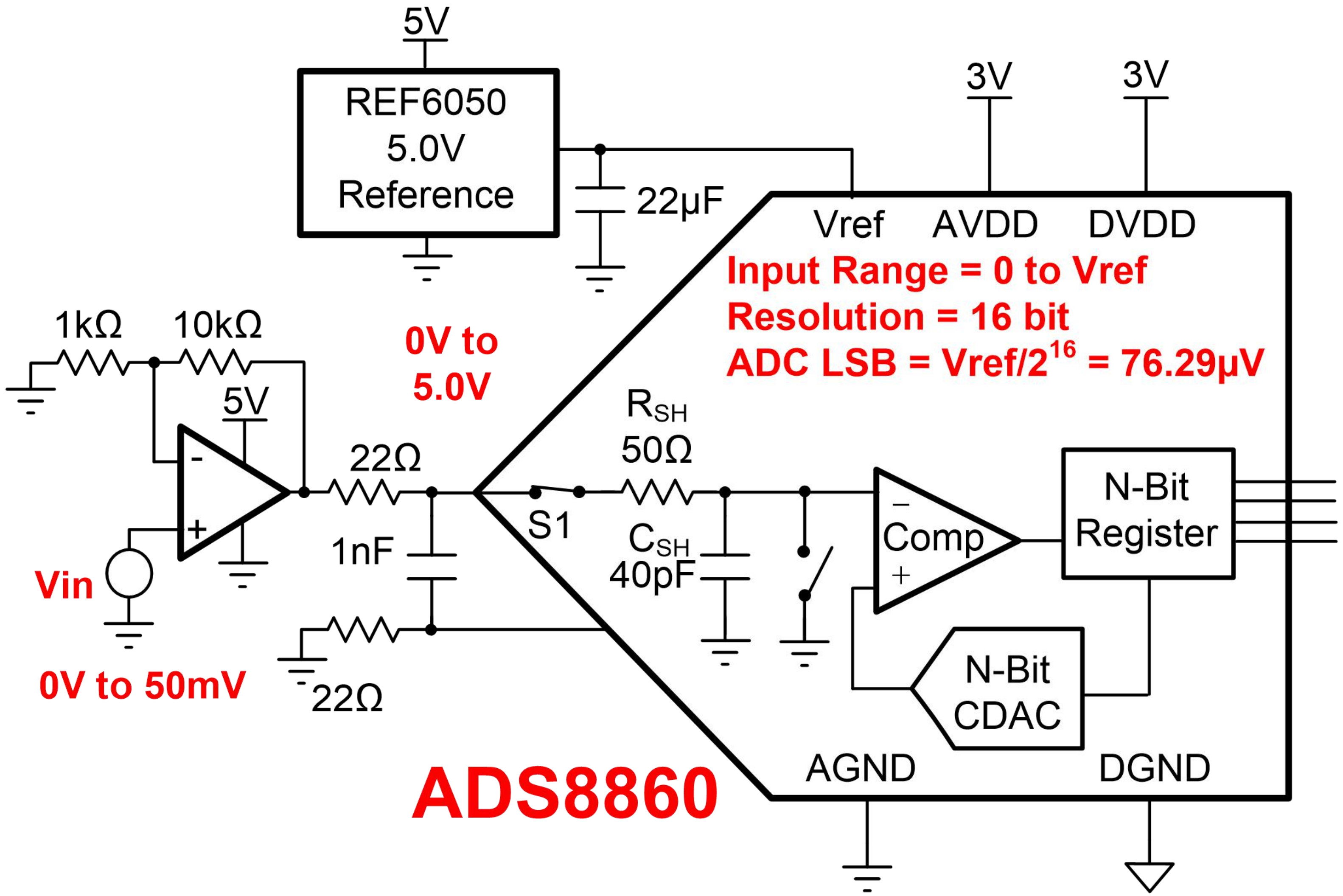
Click here to access Excel Spreadsheet for data collection.

Your results should show the same trend as the expected result but the specific values will differ.

How Driver Noise Affecting ADC System

Speaker: Andrew Wang

SNR of Amplifier + ADC: General Equations



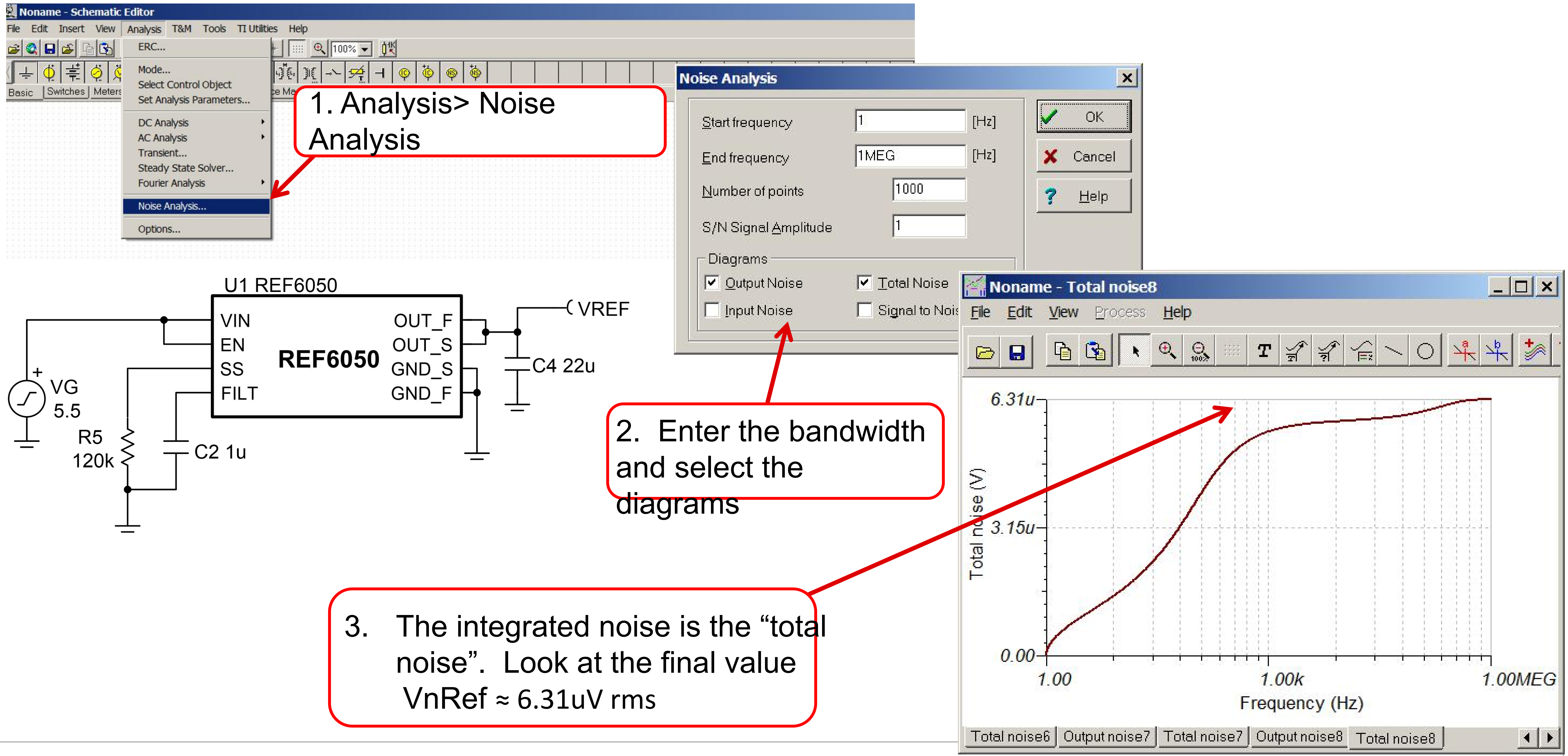
$$SNR_{ADC} = 20 \cdot \log\left(\frac{V_{FSR\_rms}}{V_{nADC}}\right)$$ Solve for noise

$$V_{nADC} = \frac{V_{FSR\_rms}}{10^{\left(\frac{SNR_{ADC}}{20}\right)}}$$ From ADC data sheet

$$V_{nT} = \sqrt{(V_{nADC})^2 + (V_{nAmp})^2 + (V_{nRef})^2}$$ Total RMS Noise

$$SNR_{total} = 20 \cdot \log\left(\frac{V_{FSR\_rms}}{V_{nT}}\right)$$ ADC+Amp+Ref

Find the REF6050 Noise

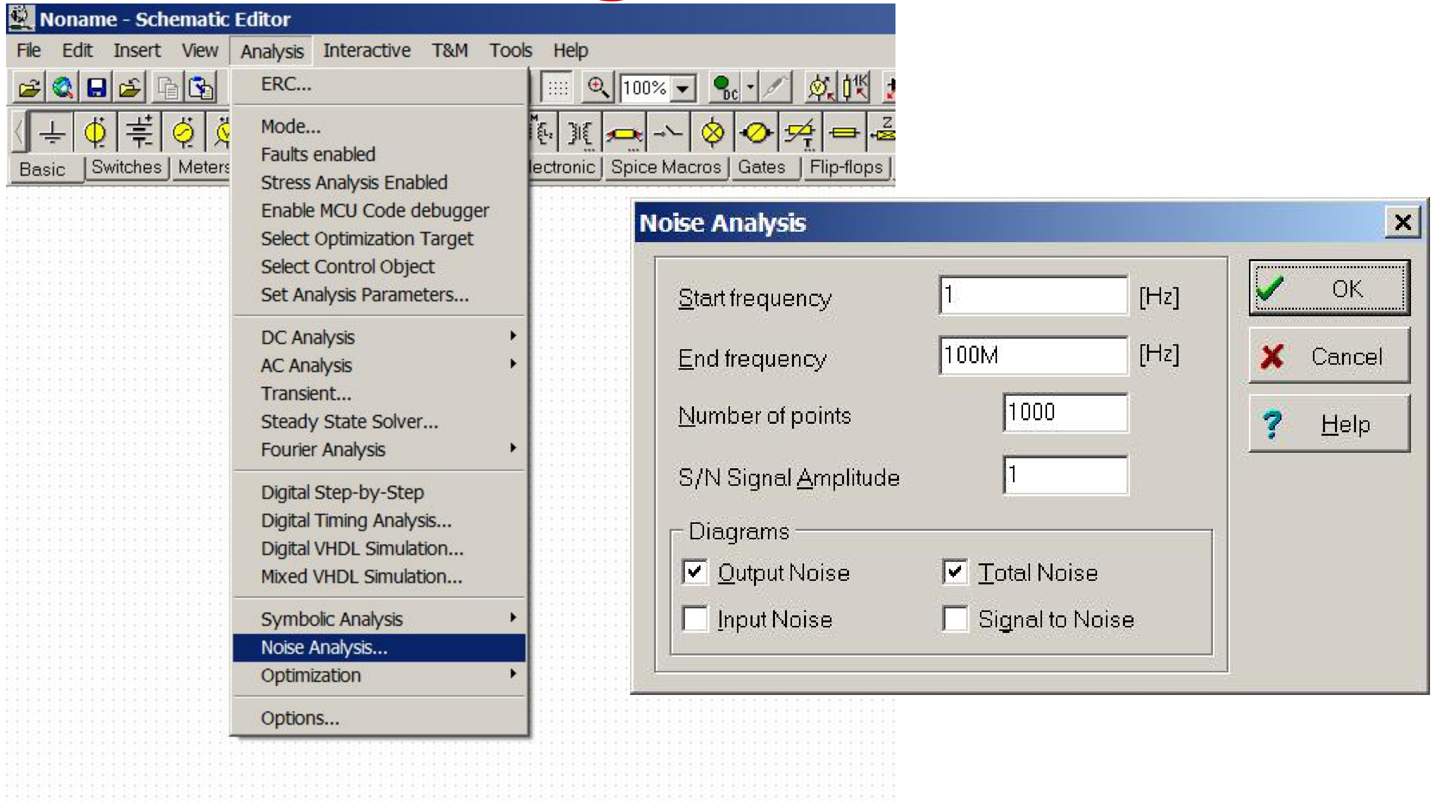


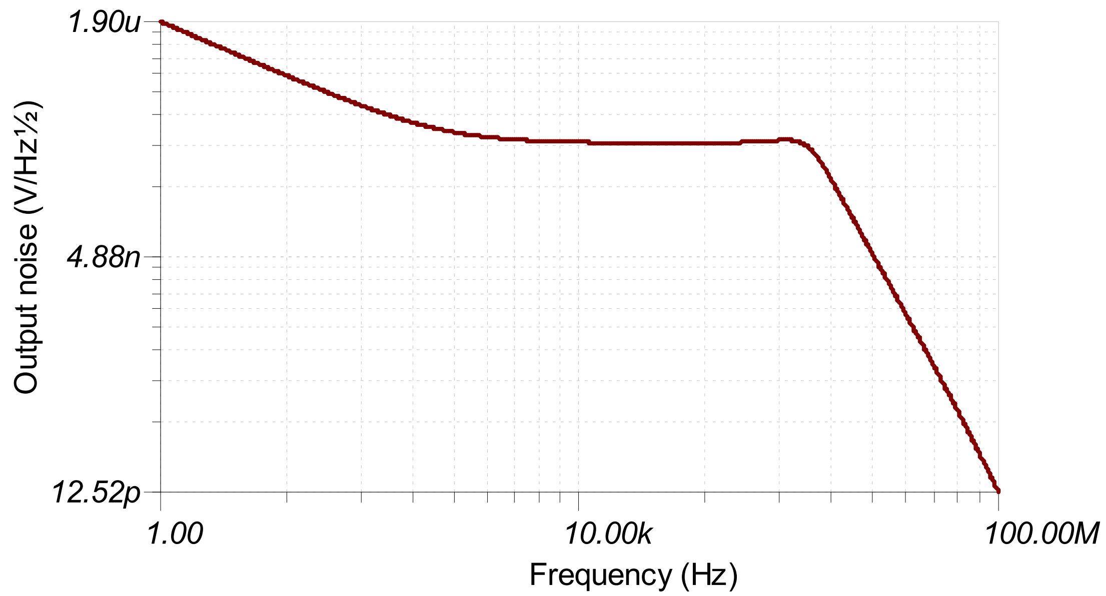
1. Analysis> Noise Analysis

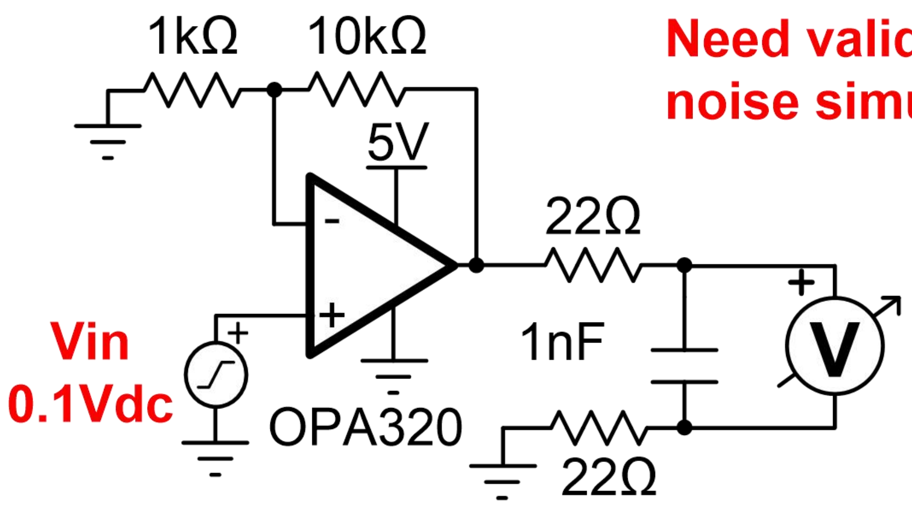
2. Enter the bandwidth and select the diagrams

3. The integrated noise is the "total noise". Look at the final value VnRef ≈ 6.31uV rms

Simulating Amplifier Noise





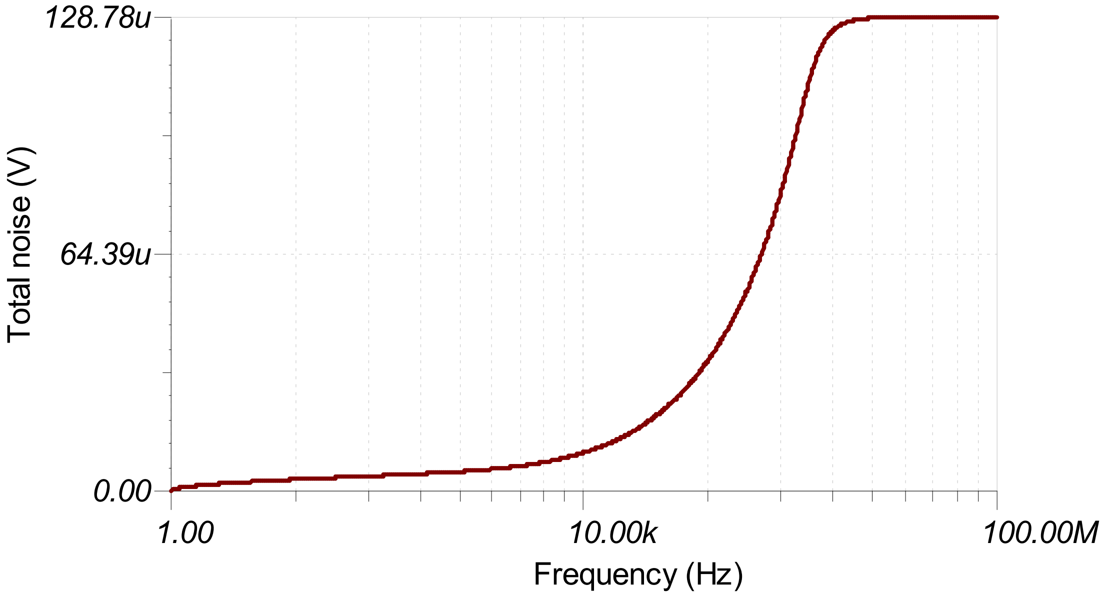


Need valid dc operating point for noise simulation!

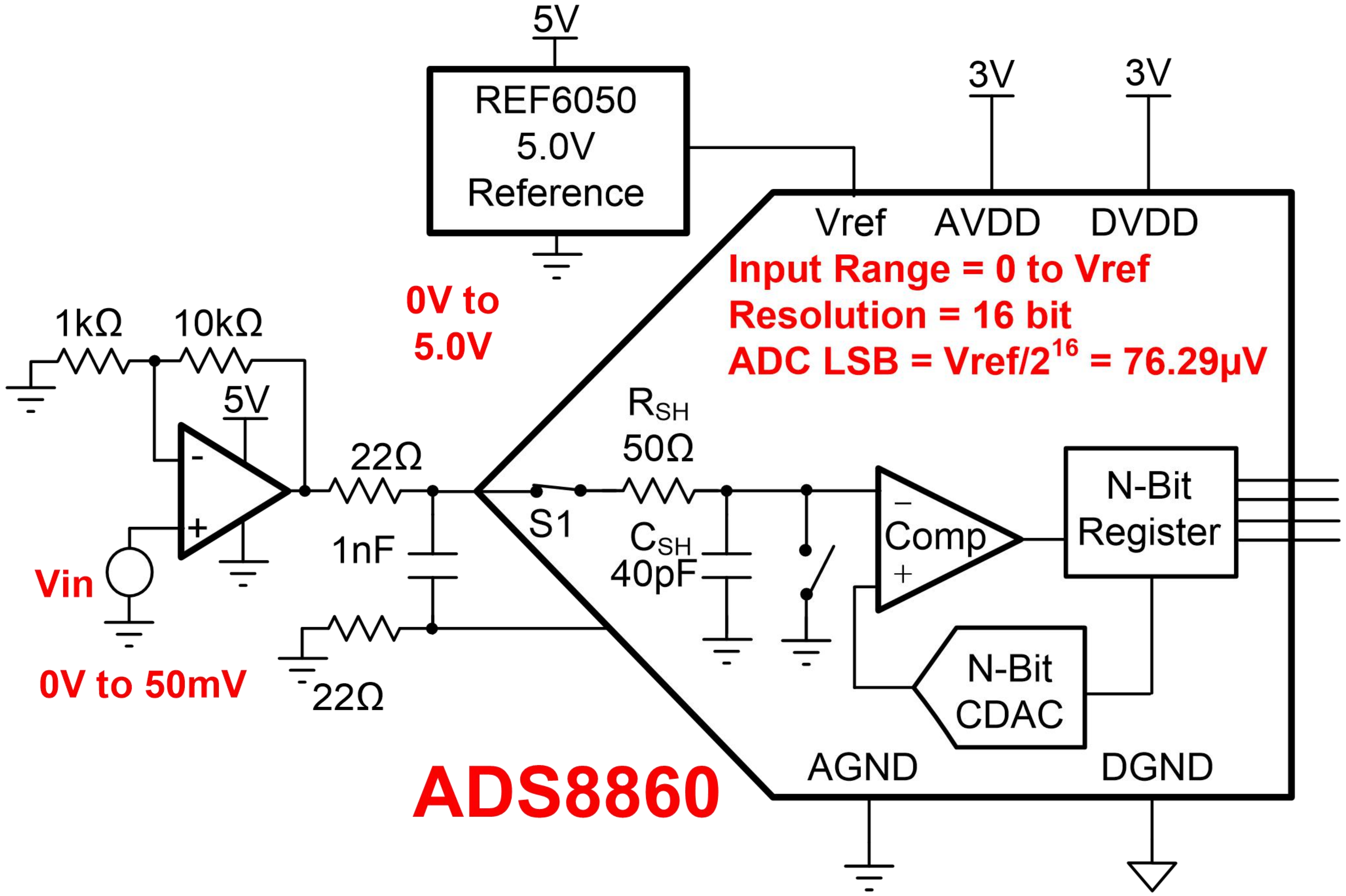
V_{outDC} = 11 x 0.1V = 1.1V

E_{nrms} = 128.8µV rms

E_{npp} = 6·128.8µV rms = 773µVpp



SNR of Amplifier + ADC: Example Calculation



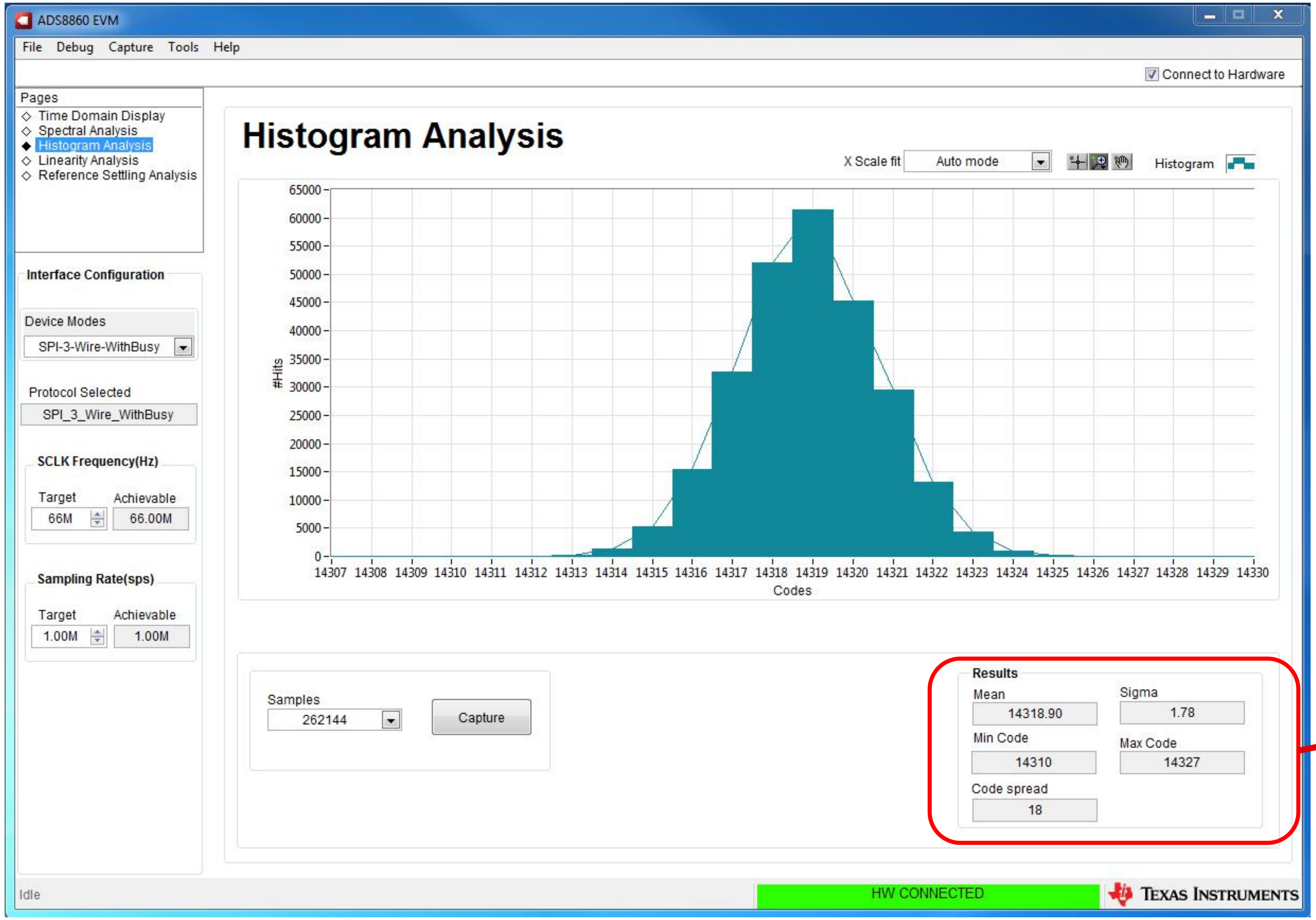
$$V_{FSR\_rms} = V_{FSRpk} \cdot 0.707$$
$$V_{FSR\_rms} = 0.5 \cdot FSR \cdot 0.707$$
$$= 0.5 \cdot 5V \cdot 0.707 = 1.767V$$

$$V_{nADC} = \frac{V_{FSR\_rms}}{10^{\left(\frac{SNR_{ADC}}{20}\right)}} = \frac{1.767V}{10^{\left(\frac{93dB}{20}\right)}} = 39.6\mu V\ rms$$

$$V_{nT} = \sqrt{(V_{nADC})^2 + \left(V_{nAmp}\right)^2 + (V_{nRef})^2}$$
$$= \sqrt{(36.9\mu V)^2 + (128.8\mu V)^2 + (6.3\mu V)^2} = 134\mu V\ rms$$

$$SNR_{total} = 20 \cdot \log\left(\frac{V_{FSR_{rms}}}{V_{nT}}\right) = 20 \cdot \log\left(\frac{1.767V}{134\mu V}\right) = 82.4\ dB$$

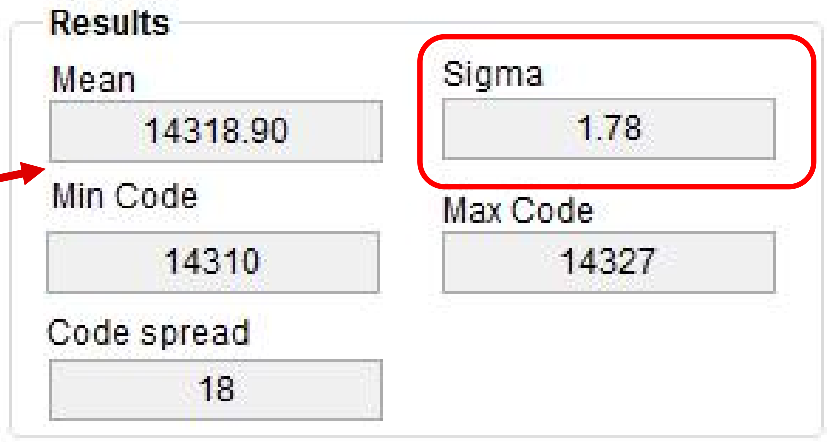
SNR of Amplifier + ADC: Measured Result



$$LSB = \frac{FSR}{2^N} = \frac{5V}{2^{16}} = 76.29\mu V$$

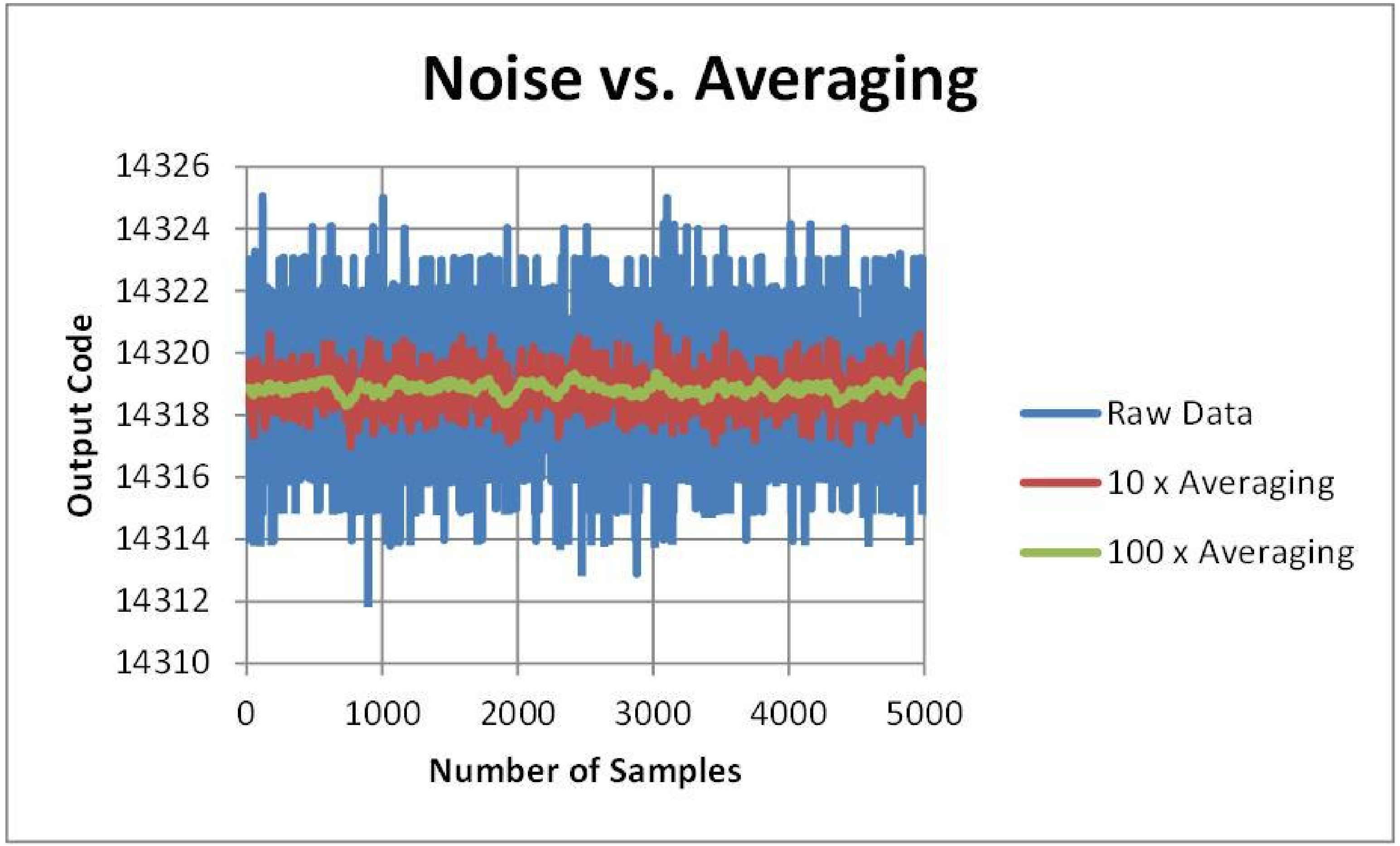
$$V_{nTmeas} = \sigma_{adc} \cdot LSB = 1.78 \cdot 76.29\mu V = 136\mu V\ rms$$

$V_{nTCalc} = 134\mu V\ rms$ *from the previous slide*



rms noise is one sigma

Averaging to Reduce Noise



Measured vs. Calculated Averaging

	Measured RMS codes	Calculated RMS codes
Standard Deviation Raw Data	1.80	na
Standard Deviation 10 x Averaging	0.59	0.57
Standard Deviation 100 x Averaging	0.18	0.18

$$V_{nAvg} = \frac{V_n}{\sqrt{N}}$$

Where
V_n *is the RMS noise*
N *is the number of averages*
V_{nAvg} *is the RMS noise after averaging*

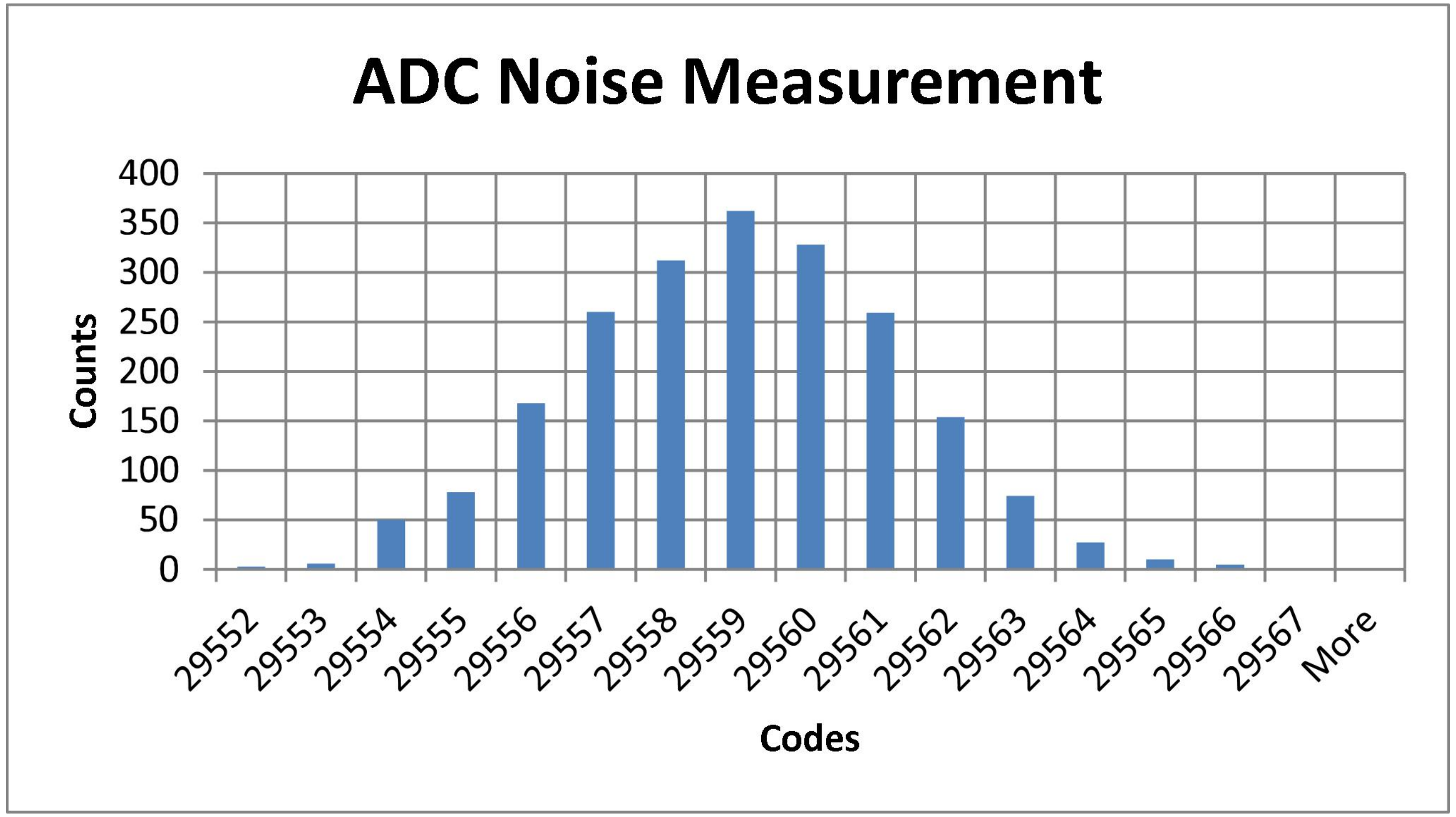
$$V_{nAvg} = \frac{V_n}{\sqrt{N}} = \frac{1.8\ codes}{\sqrt{10}} = 0.57\ codes$$

$$SNR_{avg} = 20 \cdot \log\left(\frac{V_s}{V_n/\sqrt{N}}\right) = 20 \cdot \log\left(\frac{V_s}{V_n}\right) + 10 \cdot \log(N)$$

quick quiz.

Quiz: Calculating the total noise for ADC systems

1. The histogram below was measured with a data converter:
   a) What is the RMS noise voltage?
   b) Assume the output is averaged using an 8 point rolling average. What is the averaged noise?



FSR = ±5V
Resolution = 18
Standard Deviation=σ = 2.25 codes
Mean = 29558.4

Quiz: Calculating the total noise for ADC systems

1. The histogram below was measured with a data converter:
   a) What is the RMS noise voltage? **ANS: 85.83µV rms**
   b) Assume the output is averaged using a 8 point rolling average. What is the averaged noise? **ANS: 30.35µV**

FSR = ±5V
Resolution = 18
Standard Deviation=σ = 2.25 codes
Mean = 29558.4

RMS Noise Voltage

$$V_{osT} = E_{R1} + E_{GU1} + E_{GU3}$$

$$V_{osT} = 0.1\% + 0.6\% + 0.01\% = \pm 0.71\%$$

Statistical Worse Case Gain Error

Output With 8 point rolling average

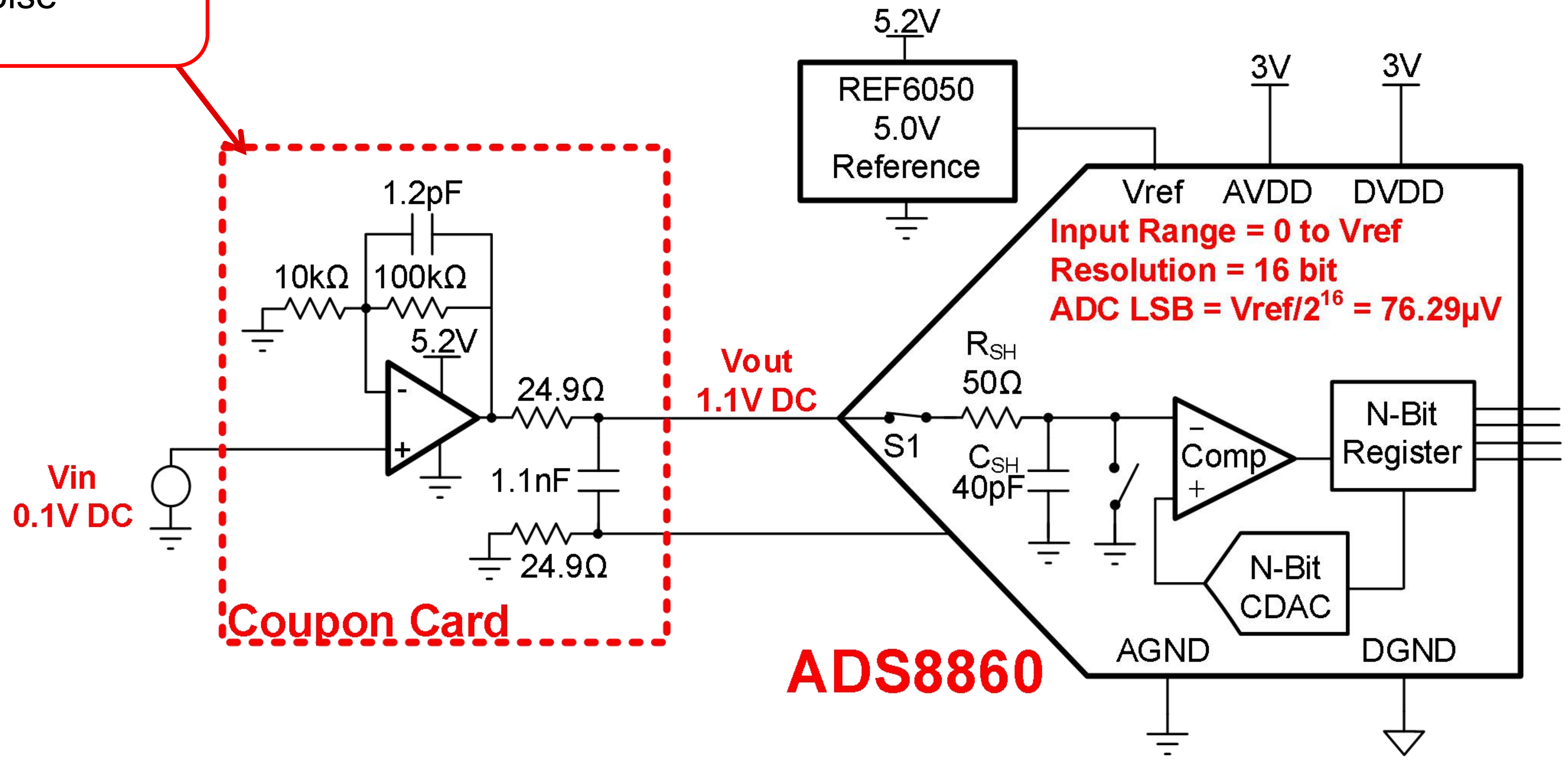
$$V_{osT} = \sqrt{(E_{R1})^2+(E_{GU1})^2+(E_{GU3})^2}$$

$$V_{osT} = \sqrt{(0.1\%)^2+(0.6\%)^2+(0.01\%)^2} = \pm 0.608\%$$

ADC Noise Experiment

System we are Analyzing and Measuring

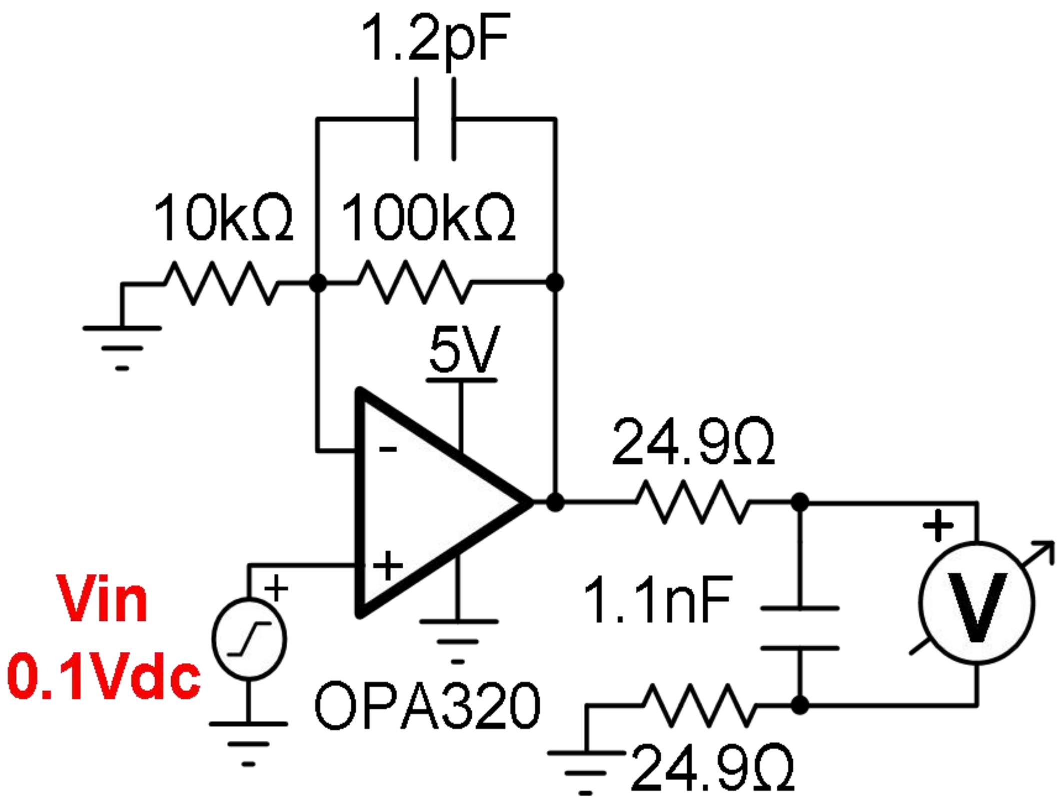
We will use two different "Coupon Cards". Each will have different noise characteristics..



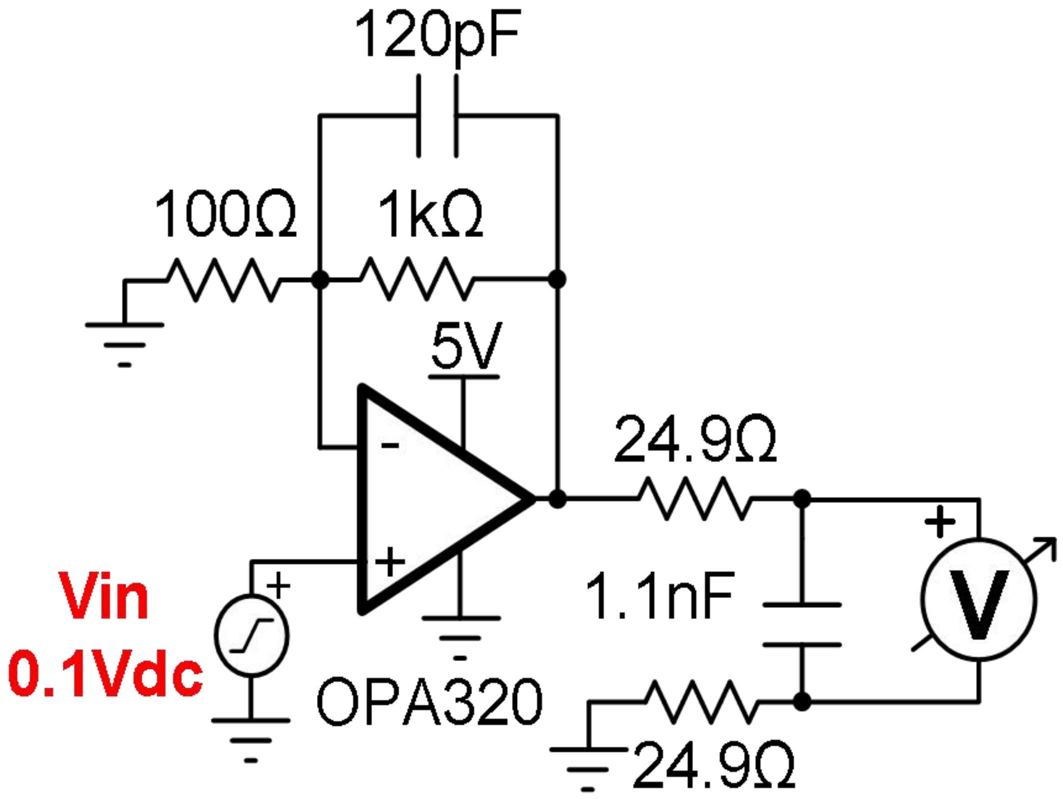
Noise1 vs Noise2 Setup

- Both circuits have the same: gain, bandwidth, and output filter
- The difference is feedback network resistance is scaled by a factor of 100
- The objective is to see how thermal noise from feedback impacts overall noise

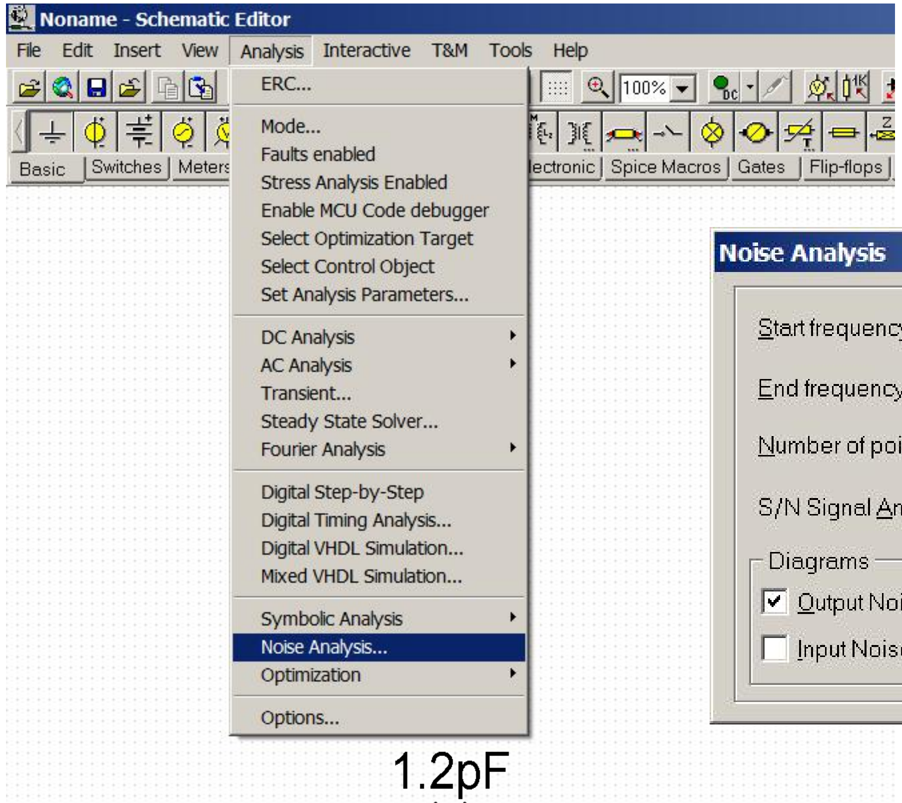
Noise 1

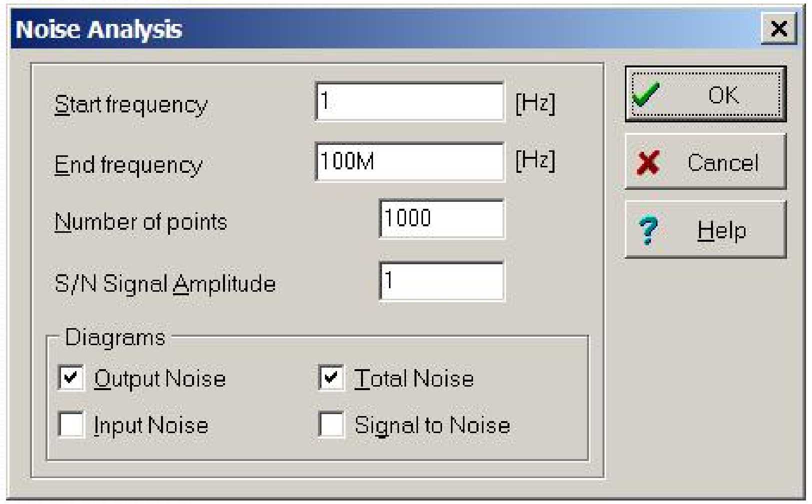


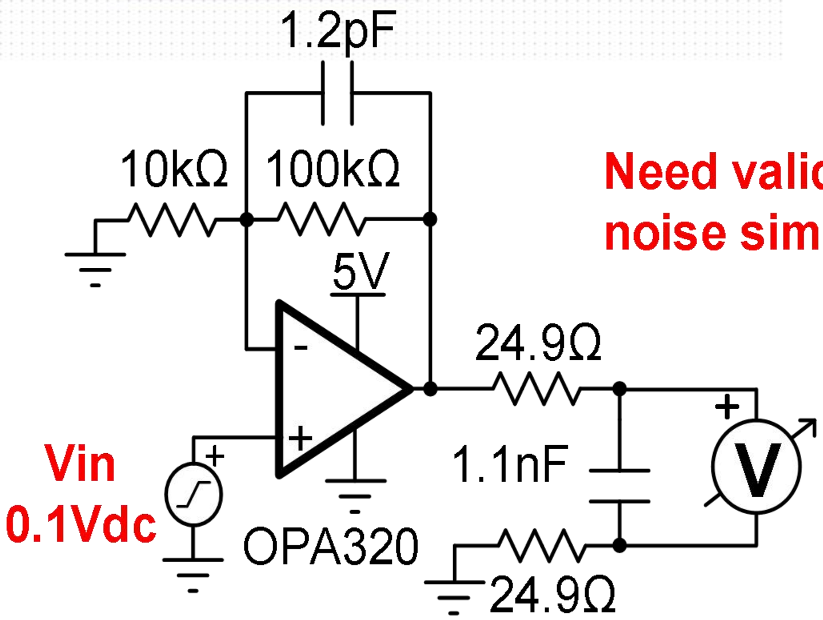
Noise 2



Simulation of Noise1





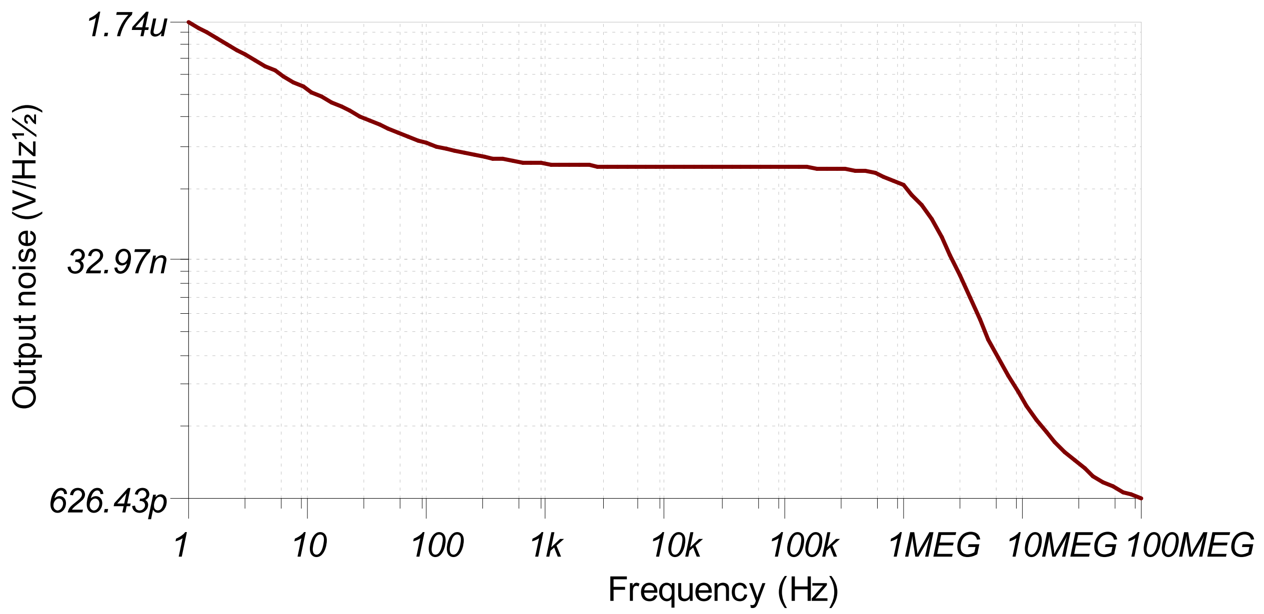


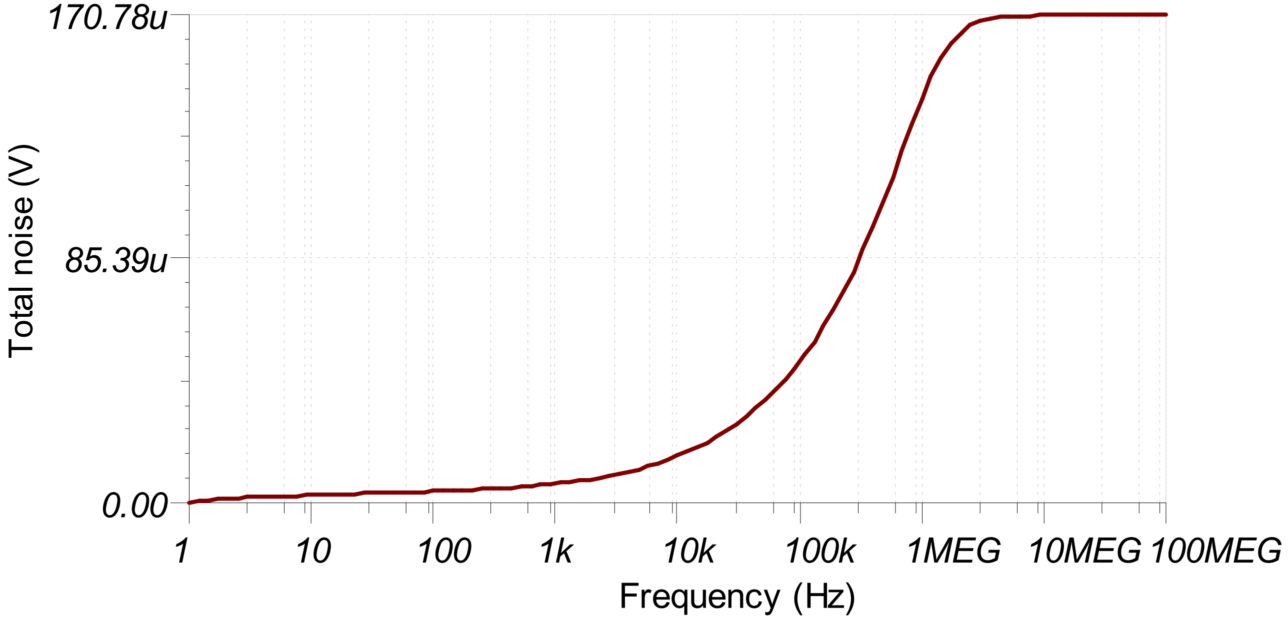
Need valid dc operating point for noise simulation!

$V_{outDC} = 11 \times 0.1V = 1.1V$

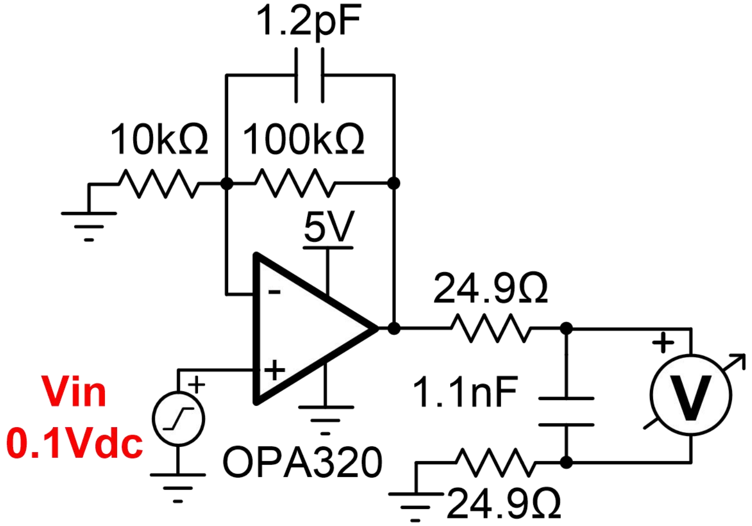
$E_{nrms} = 170.8\mu V$ rms

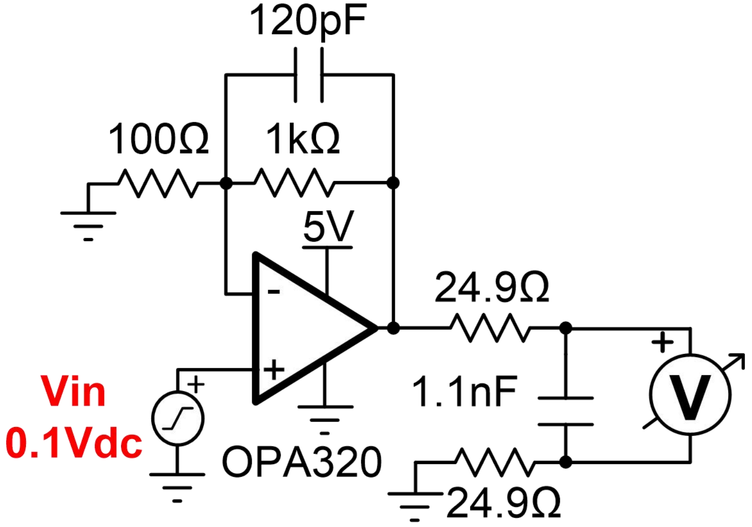
$E_{npp} = 6 \cdot 170.8\mu V$ rms $= 1.03mVpp$





Noise 1 vs Noise 2

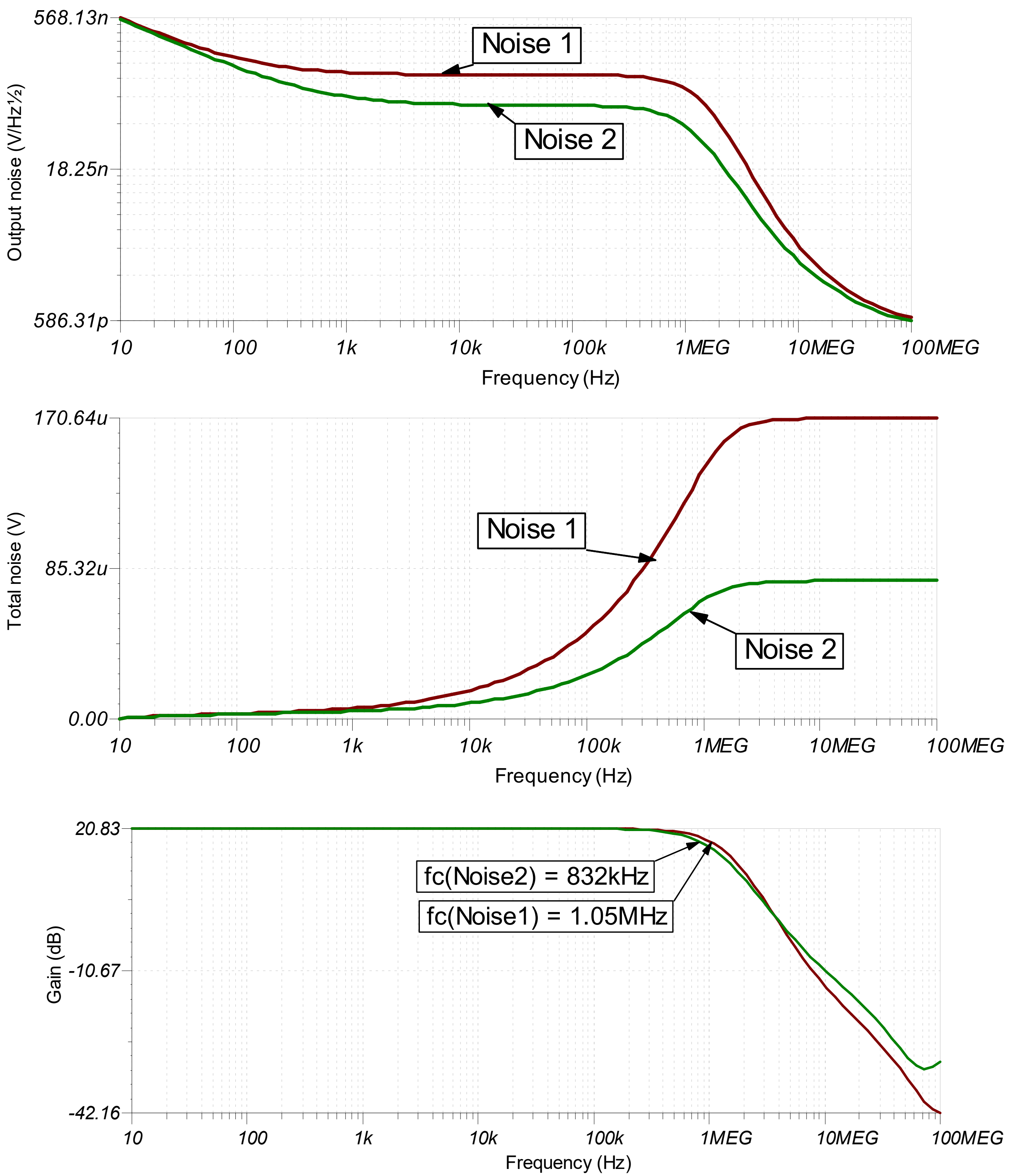




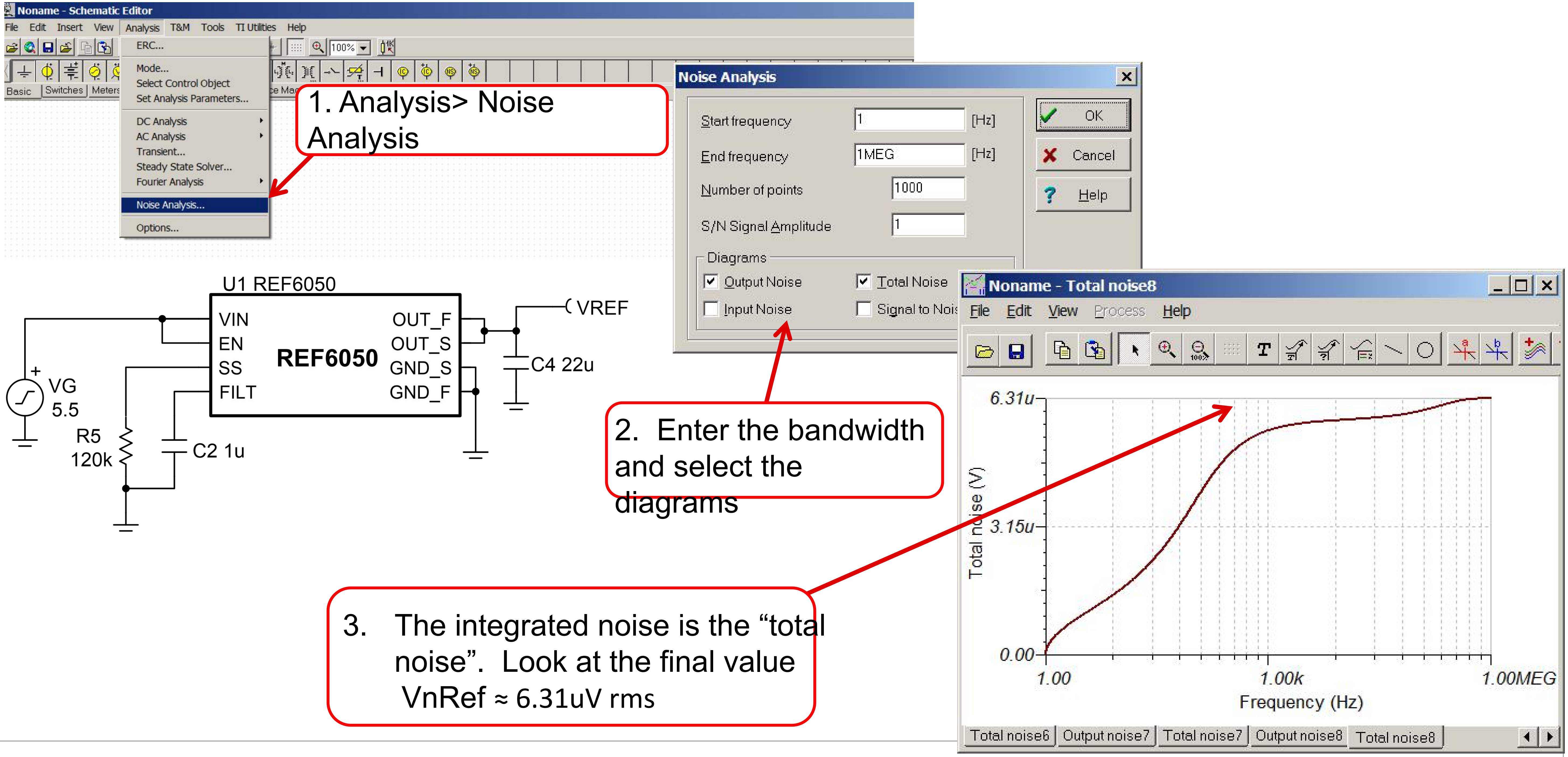
OPA320_Noise1.TSC

Click to access TINA simulation.

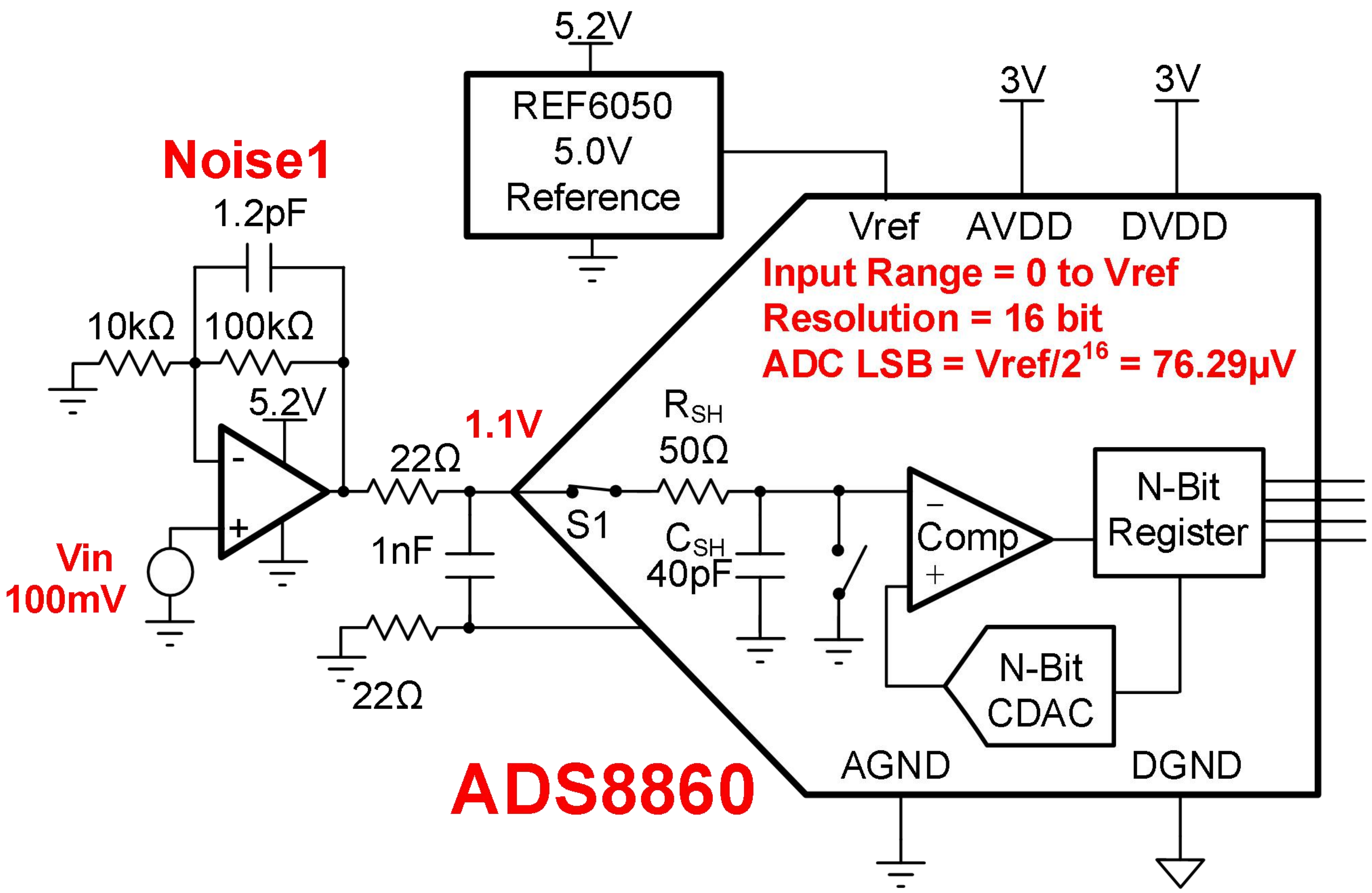
OPA320_Noise2.TSC



Find the REF6050 Noise



Total System Noise for OPA320_Noise1



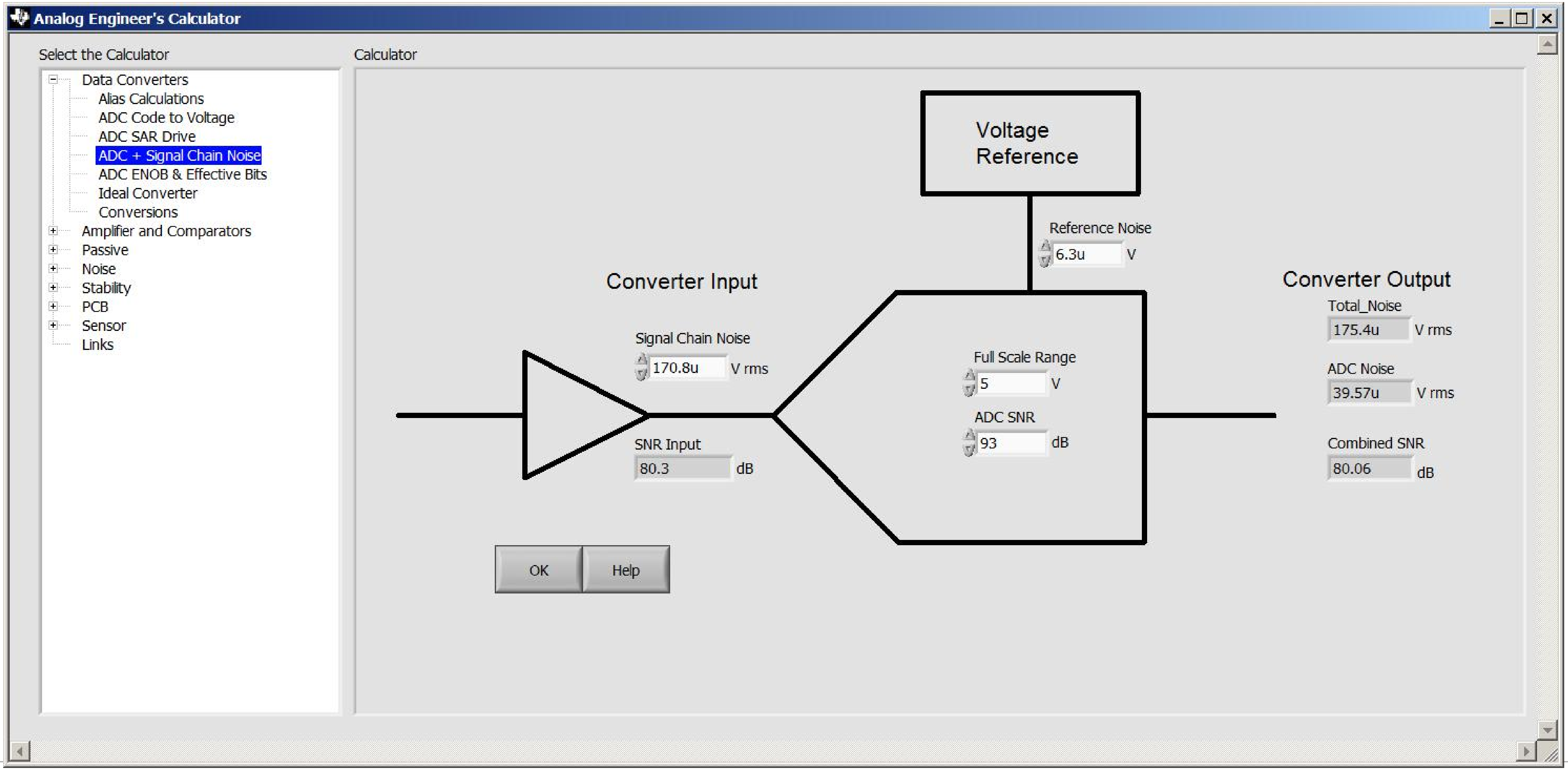
$$V_{FSR\_rms} = V_{FSRpk} \cdot 0.707$$
$$V_{FSR\_rms} = 0.5 \cdot FSR \cdot 0.707$$
$$= 0.5 \cdot 5V \cdot 0.707 = 1.767V$$

$$V_{nADC} = \frac{V_{FSR\_rms}}{10^{\left(\frac{SNR_{ADC}}{20}\right)}} = \frac{1.767V}{10^{\left(\frac{93dB}{20}\right)}} = 39.6\mu V\ rms$$

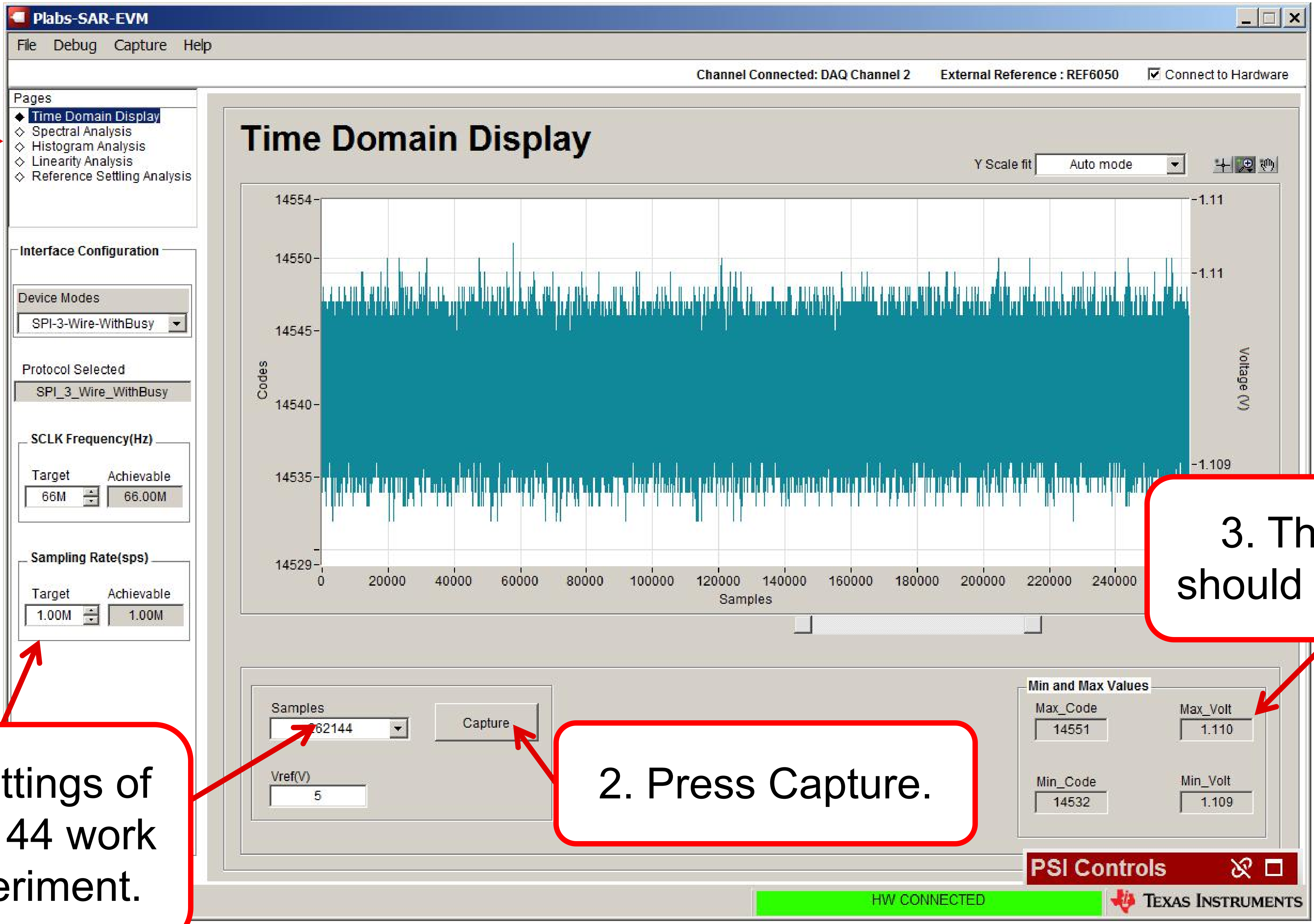
$$V_{nT} = \sqrt{(V_{nADC})^2 + (V_{nAmp})^2 + (V_{nRef})^2}$$
$$= \sqrt{(39.6\mu V)^2 + (170.8\mu V)^2 + (6.3\mu V)^2} = 175.4\mu V\ rms$$

$$SNR_{total} = 20 \cdot \log\left(\frac{V_{FSR_{rms}}}{V_{nT}}\right) = 20 \cdot \log\left(\frac{1.767V}{175.4\mu V}\right) = 80.1\ dB$$

Solve Using the Analog Engineer's Calculator



Measure the Noise and DC Level



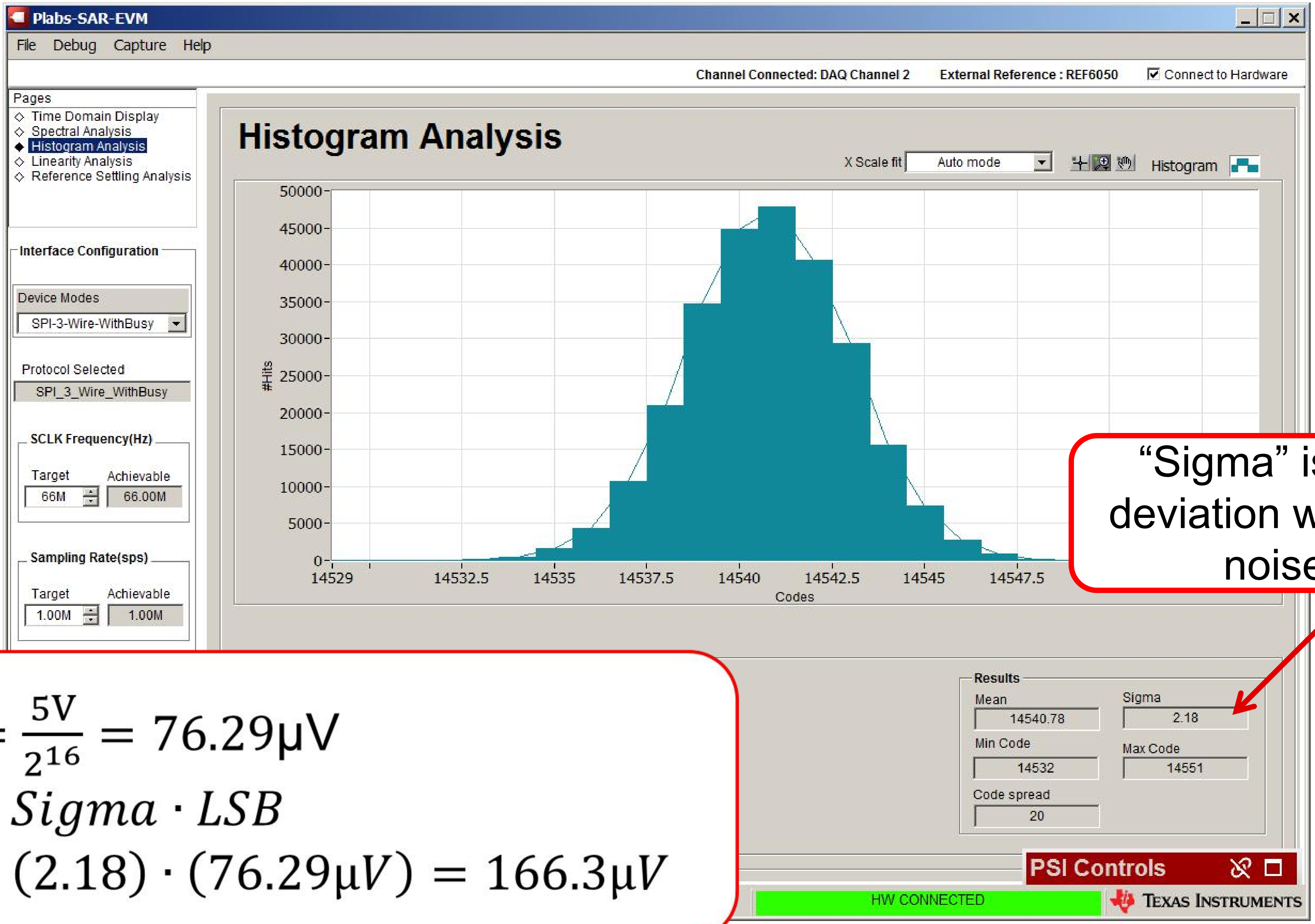
4. Change page to "Histogram Analysis"

3. The DC output should be about 1.1V.

2. Press Capture.

1. The default settings of 1Msps, and 262144 work well for this experiment.

Look at the Statistics Under "Histogram Analysis"



"Sigma" is one standard deviation which is the RMS noise in codes.

$$LSB = \frac{V_{FSR}}{2^N} = \frac{5V}{2^{16}} = 76.29\mu V$$

$$V_{noise\_meas} = Sigma \cdot LSB$$

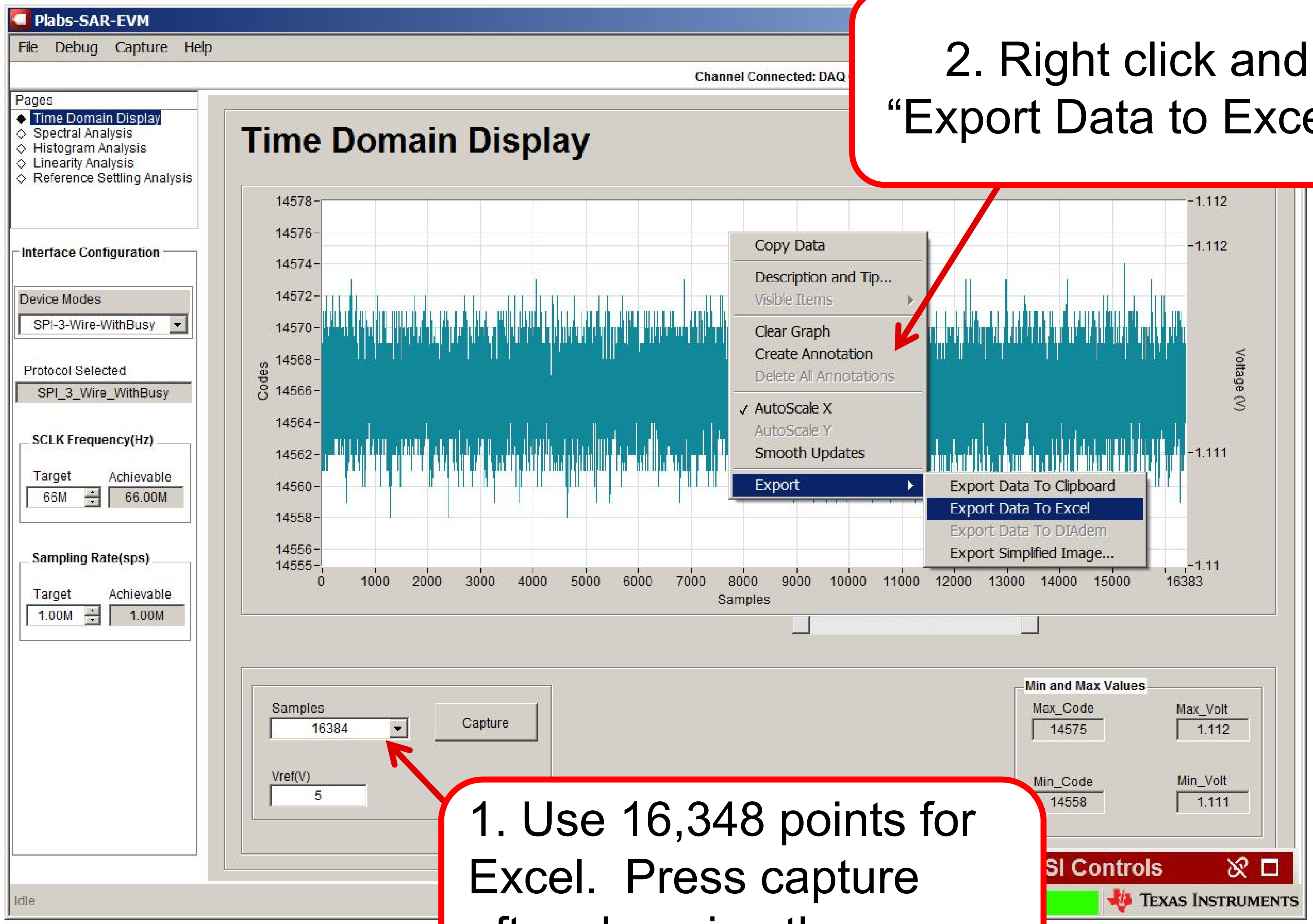
$$V_{noise\_meas} = (2.18) \cdot (76.29\mu V) = 166.3\mu V$$

2b:Measured vs Expected Results

		Vin = 0.1V DC, fsamp = 1MHz, Vref =5V, LSB = 76.29uV					
Device	**Hand Calc**	**Simulated**				**Example Measurements**	
	Amp Noise (uV)	Amp Noise (uV)	ADC Noise (uV)	Ref Noise (uV)	Total Noise (uV)	Sigma	Noise (uV)
Noise1	196.7	170.8	39.6	11.2	175.4	2.18	166.3
Noise2	99.1	78.8	39.6	11.2	88.4	1.16	88.5

Demo – Driver Noise Difference

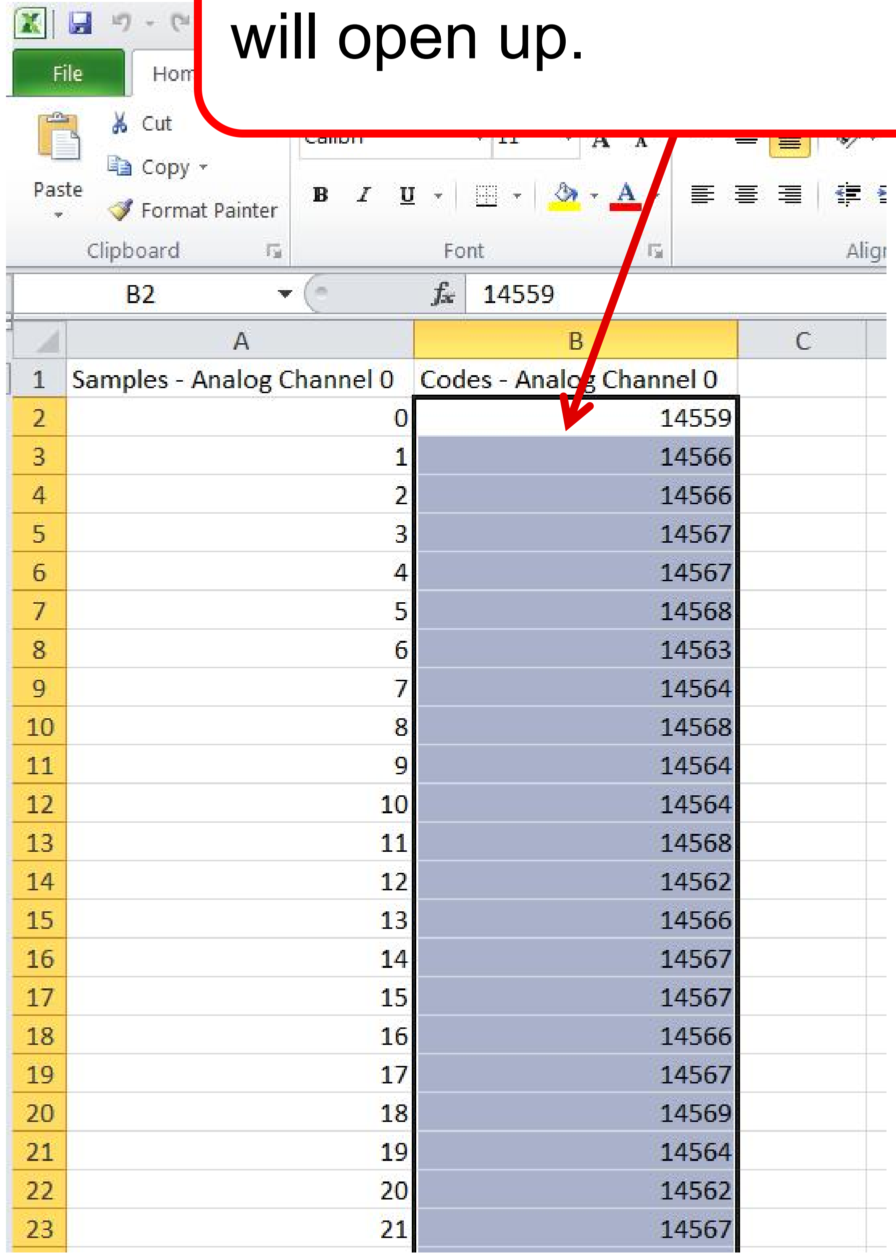
Export Data to Excel



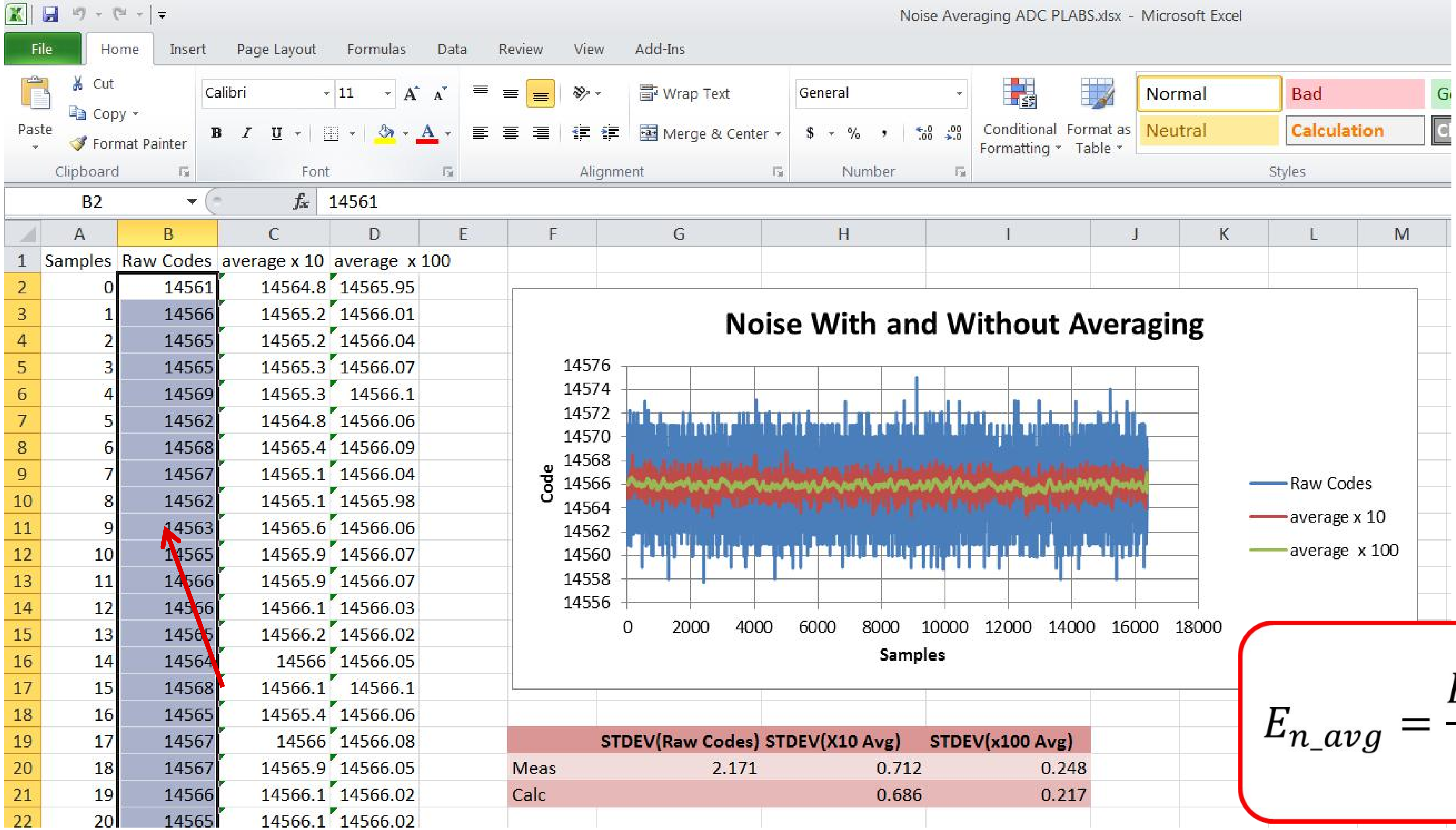
2. Right click and "Export Data to Excel".

1. Use 16,348 points for Excel. Press capture after changing the number of samples.

3. An Excel spreadsheet will open up.



Paste Your Results Under “Raw Codes”



Click to access Excel Spreadsheet.

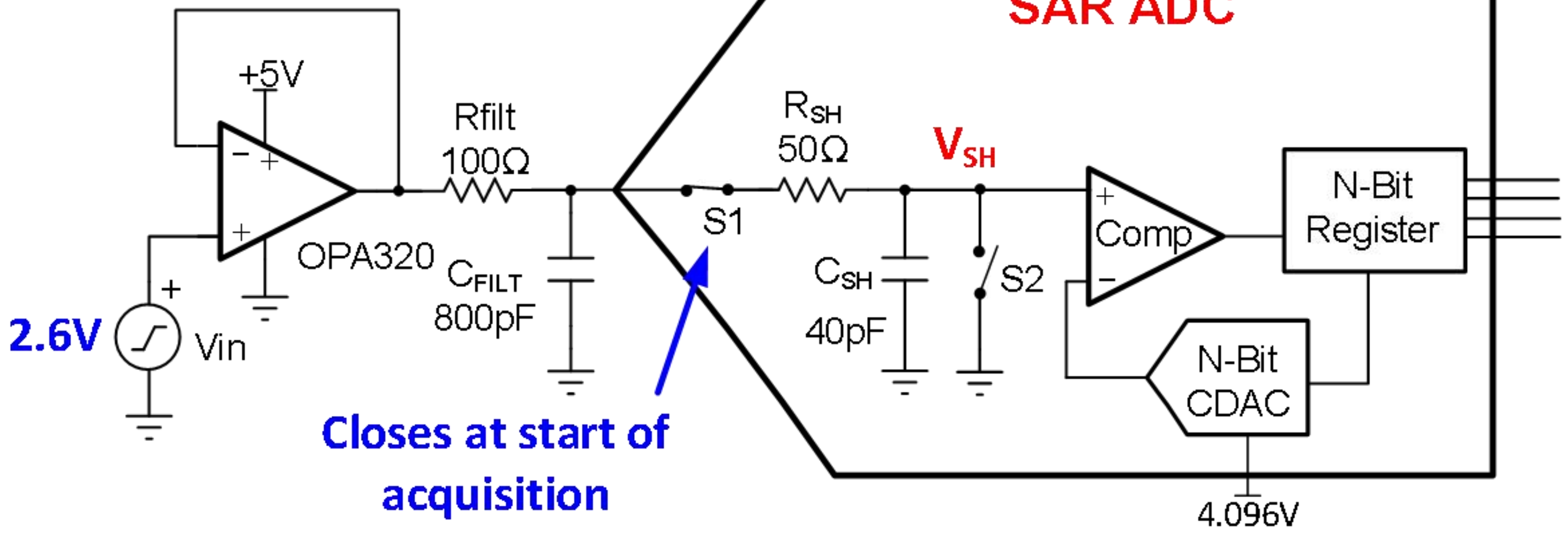
Microsoft Excel Worksheet

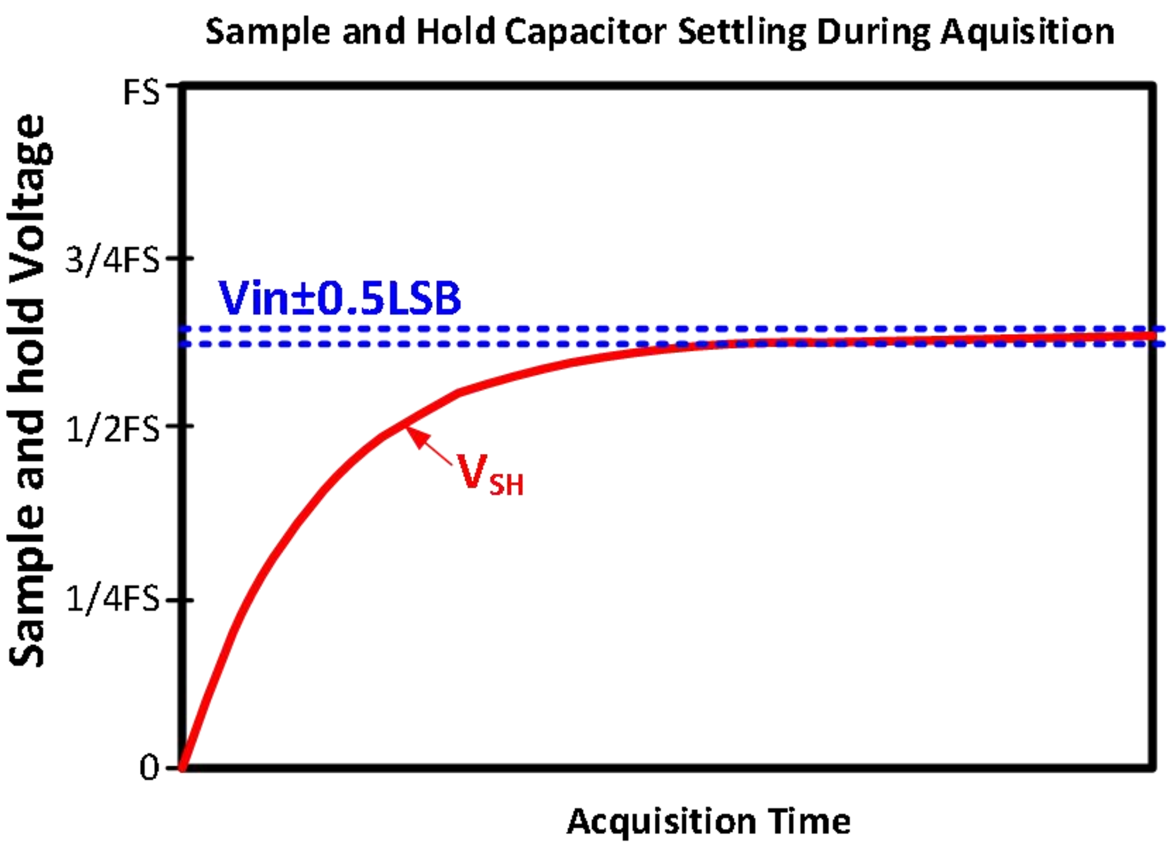
$$E_{n\_avg} = \frac{E_{n\_raw}}{\sqrt{N}}$$

SAR ADC Driver RC Optimization

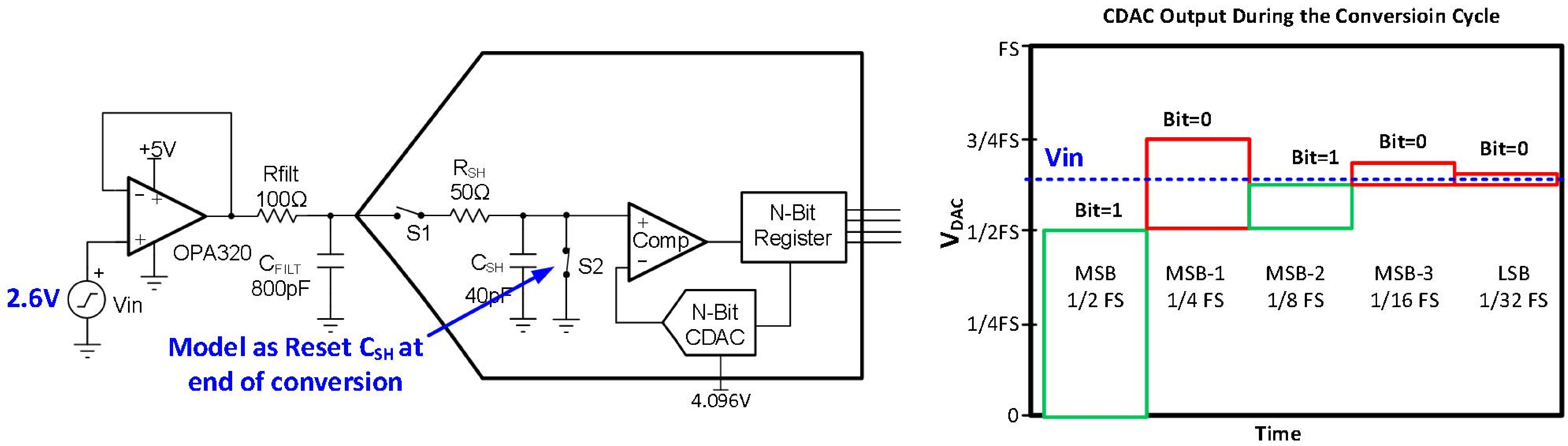
Speaker: Andrew Wang

Acquisition phase



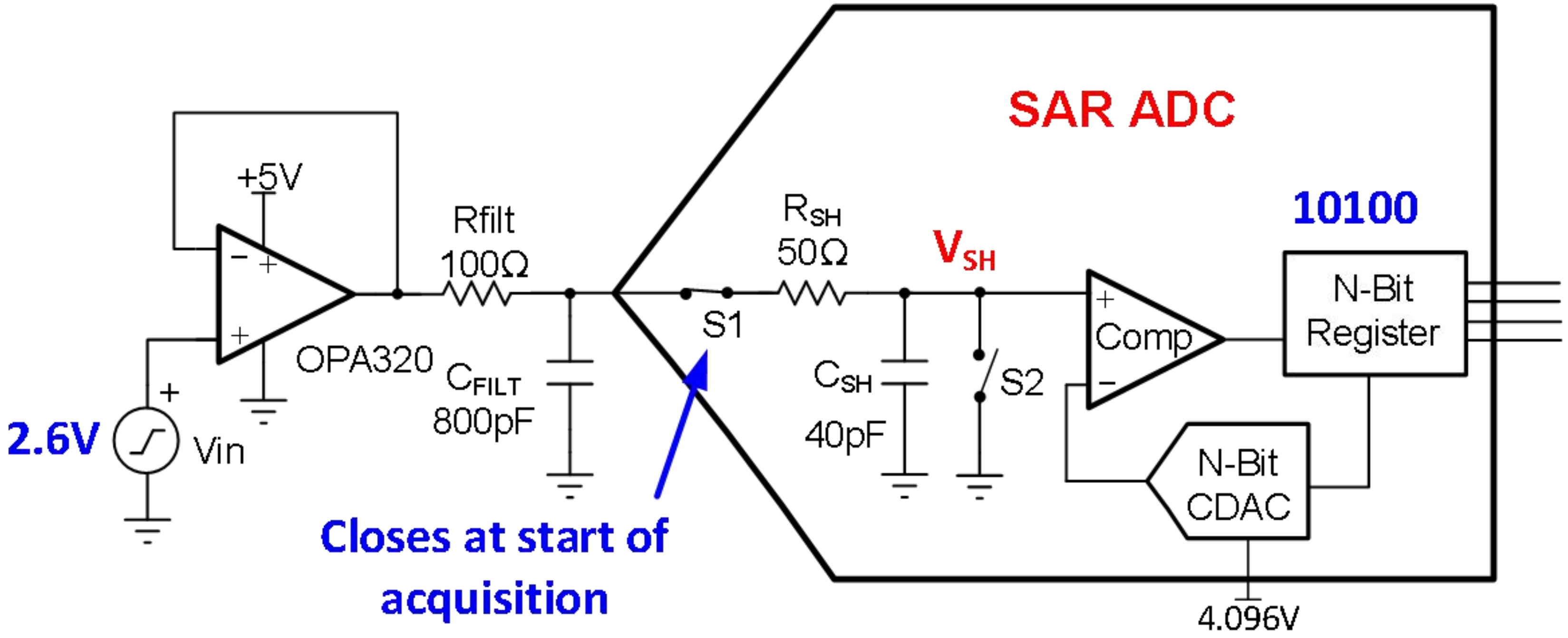


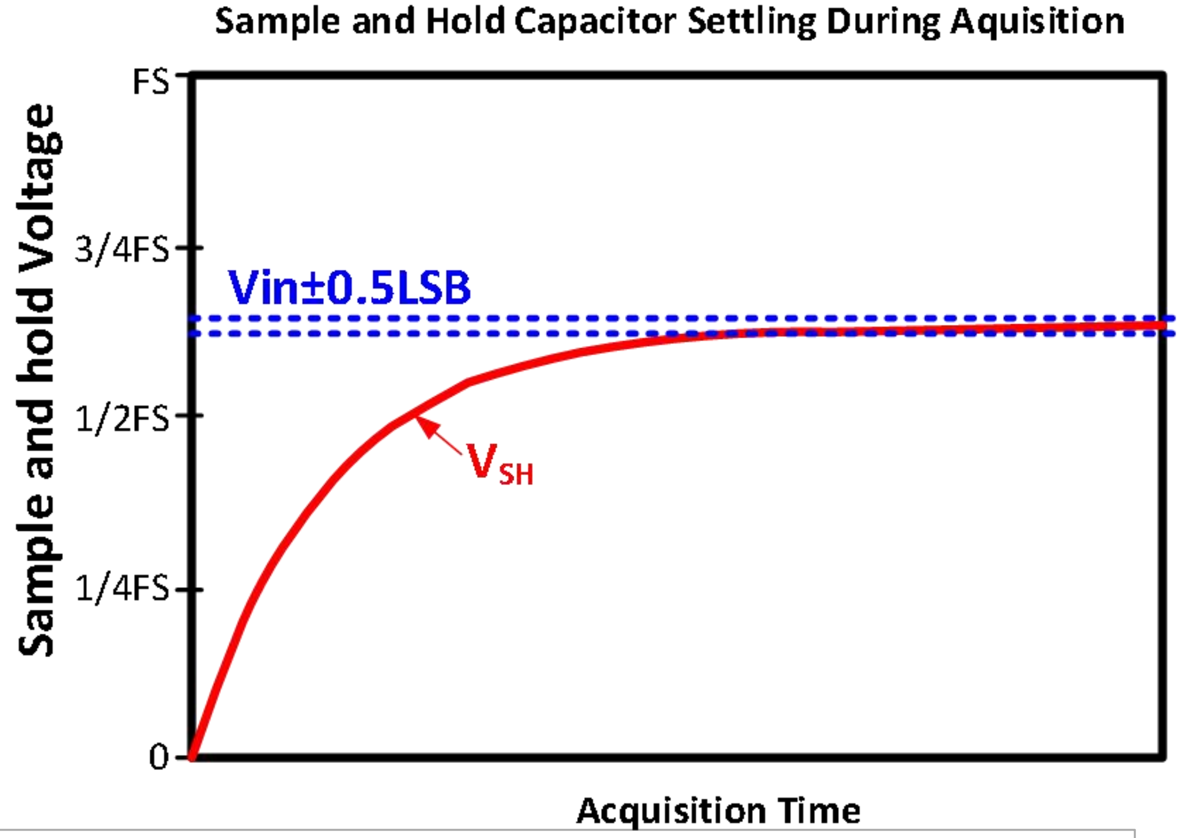
Conversion Phase



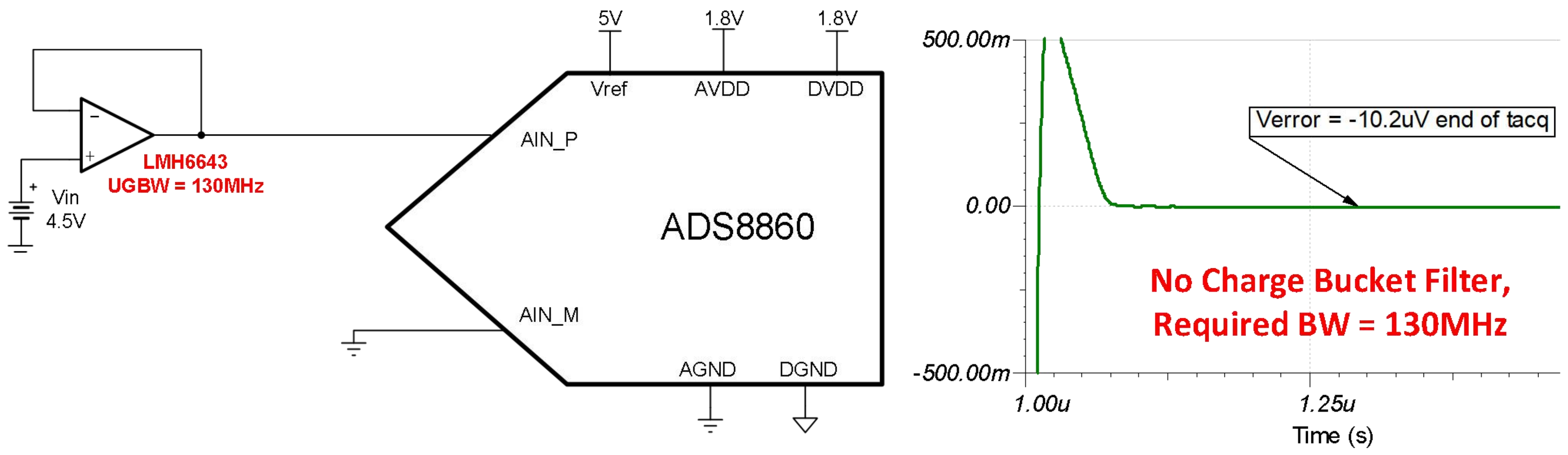
Overall Objective

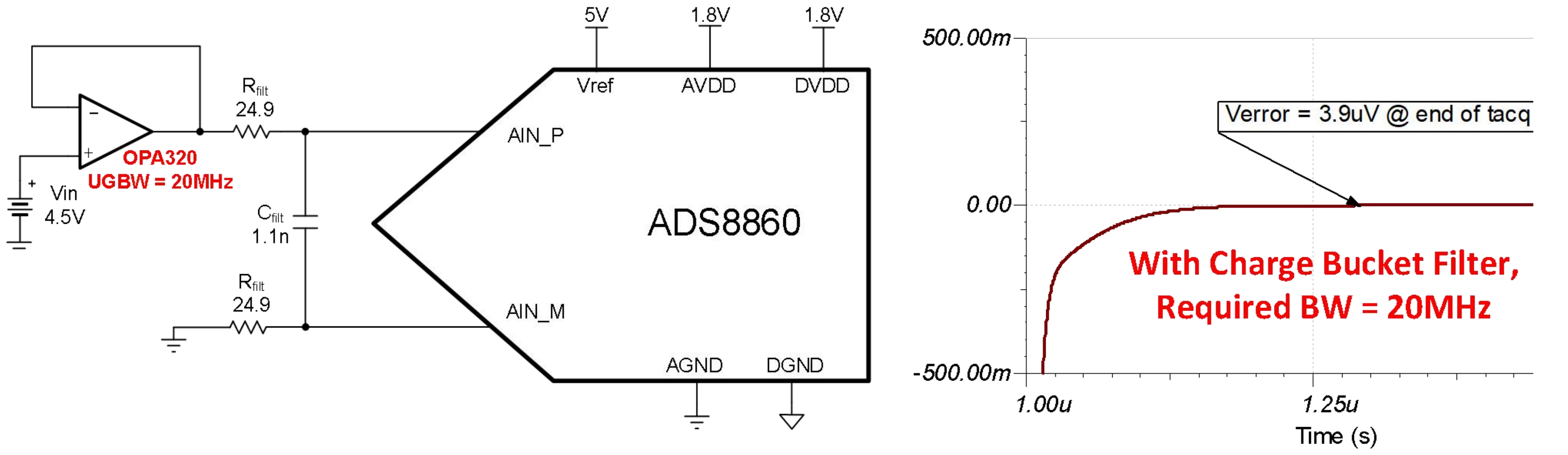
- Find Rfilt and Cfilt charge bucket filter that will optimize settling
- Find amplifier with bandwidth sufficient for settling
- Achieve final settling of 0.5LSB or better at end of tacq





Is the charge bucket filter required?

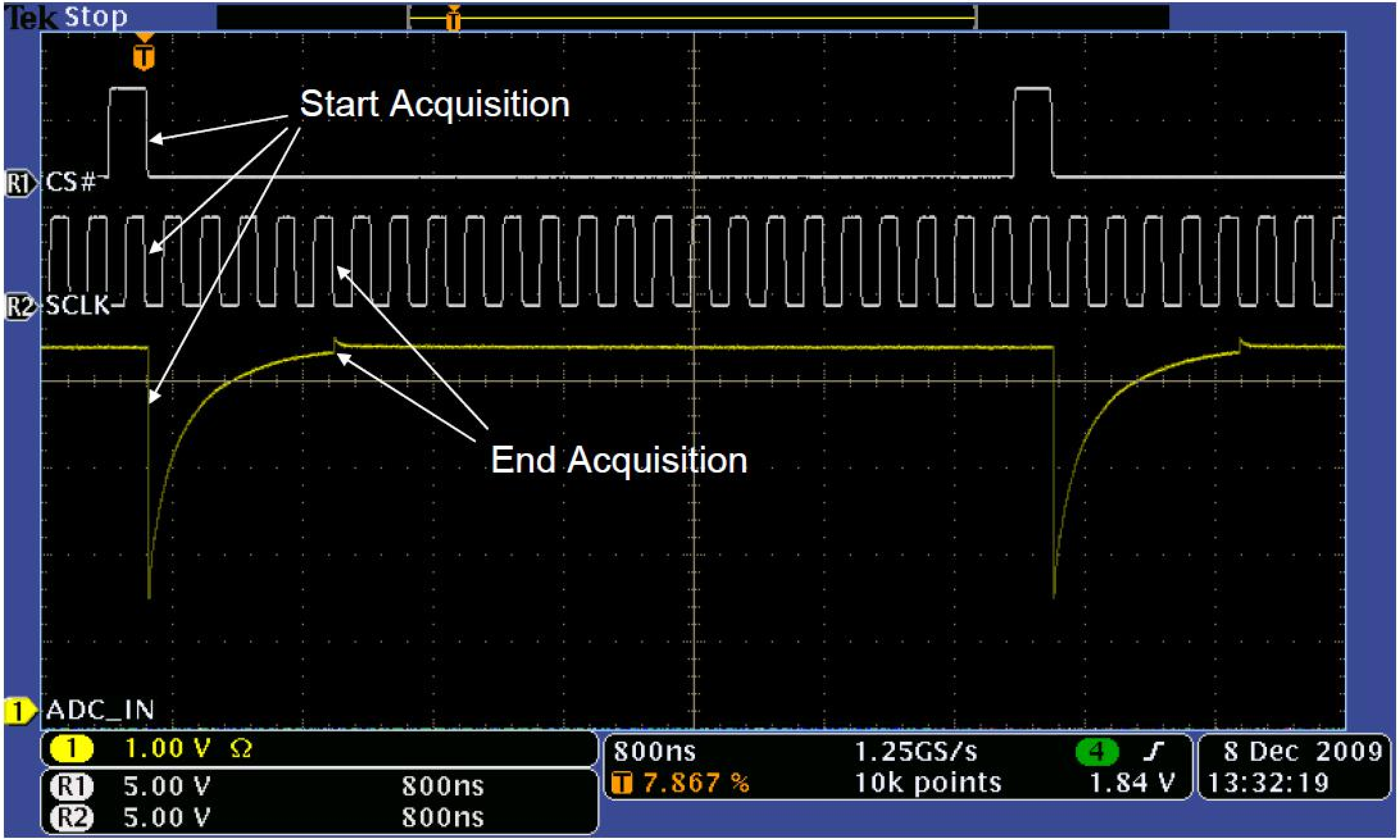




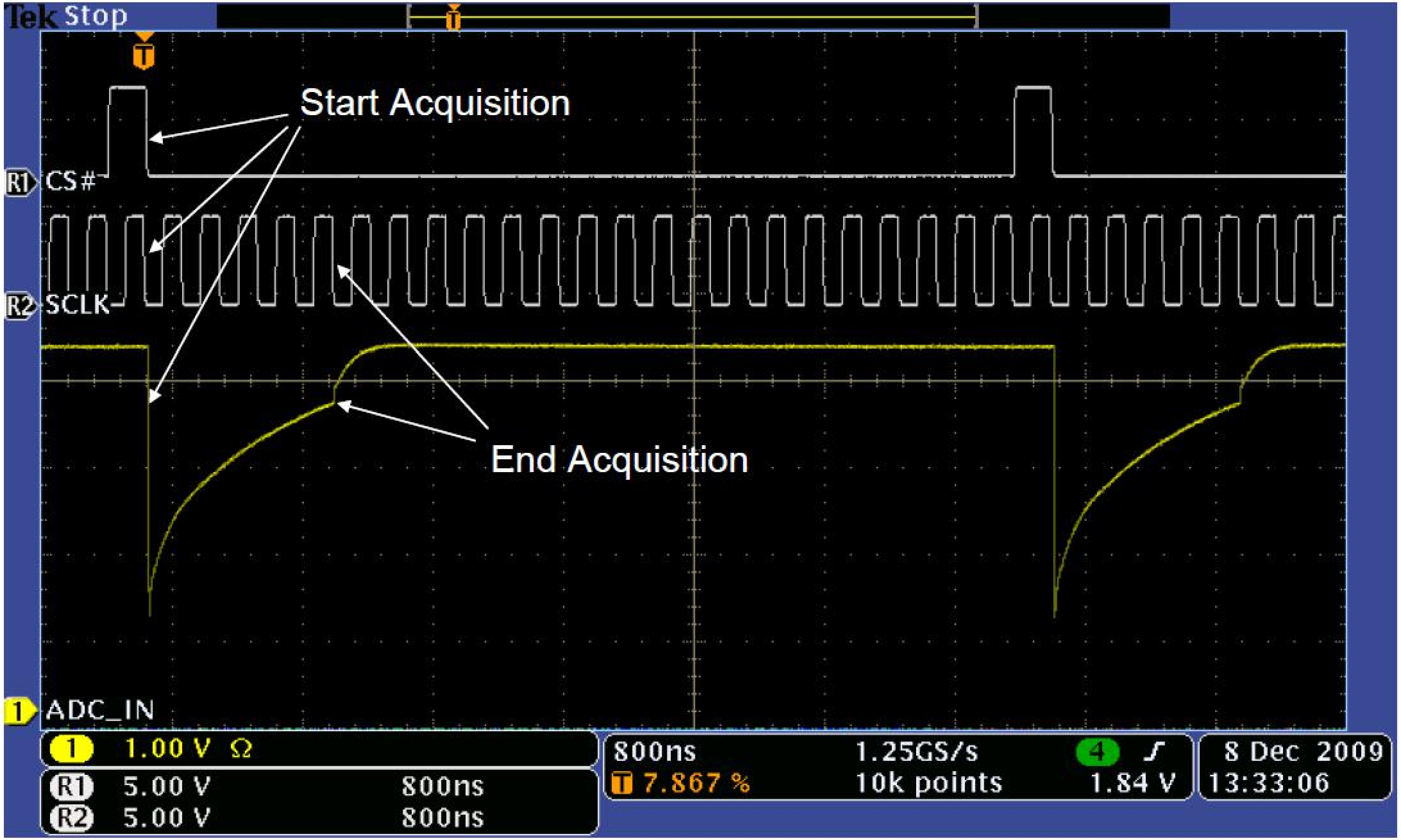
Advantage of low BW Amp

- Lower Iq
- Better Vos, Ib
- Lower cost
- Less sensitive to stability issues

ADC Input With Proper RC Filter



ADC Input With Wrong RC Filter



Example: Full Scale Range, Resolution, C_{sh}, R_{sh}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span[(1)]	AINP – AINN	0		V_{REF}	V
	Operating input range[(1)]	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		+ 0.1	V
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
	Input leakage current	During acquisition for dc input		5		nA
SYSTEM PERFORMANCE						
	Resolution			16		Bits

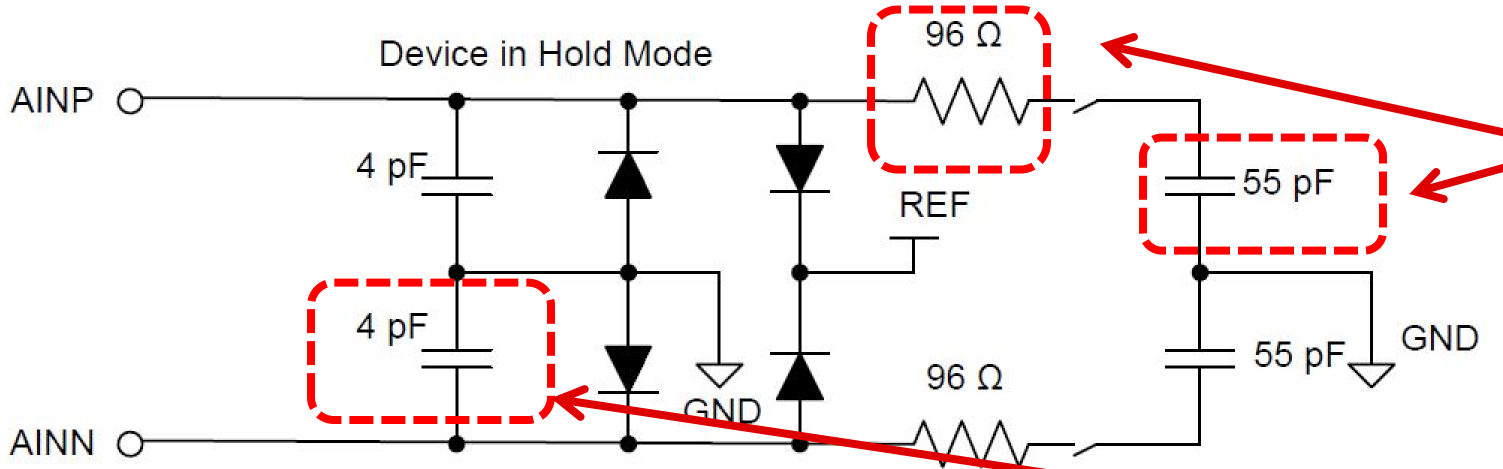


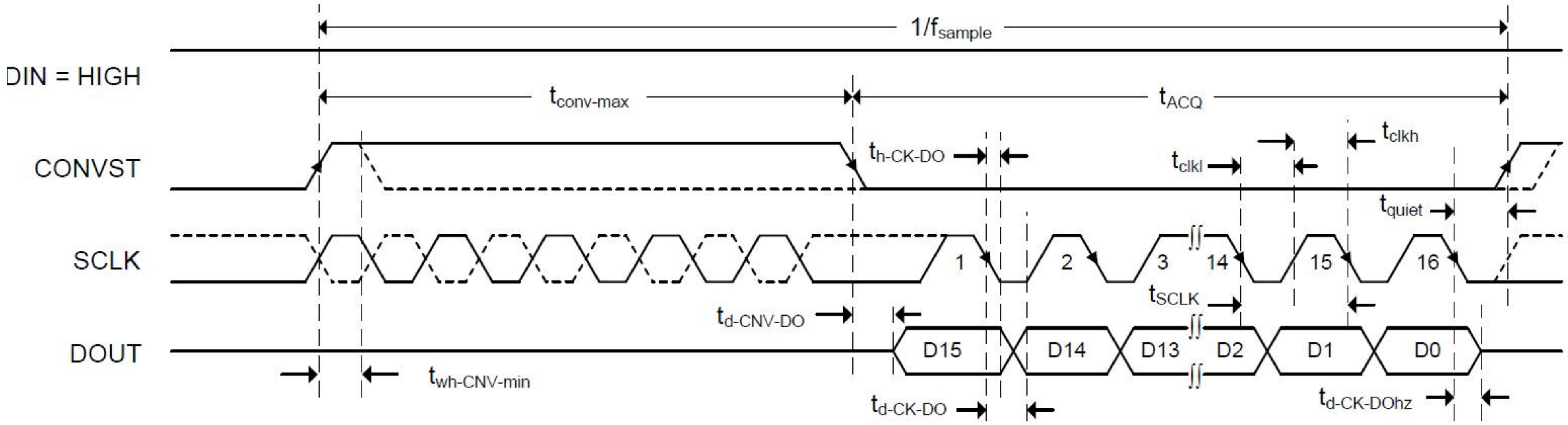
Figure 45. Input Sampling Stage Equivalent Circuit

C_{sh} and R_{sh} can usually be found in the equivalent circuit.

Full Scale Range and resolution

Note: C_I from the table
C_I = 55pF+4pF

For our example: acquisition time



Conversion time set by internal clock. The maximum time for conversion is 710ns.

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns

We are running at maximum throughput (1MHz)

$1/f_{sample} = t_{conv\text{-}max} + t_{acq\text{-}min} = 710\text{ns} + 290\text{ns} = 1\mu\text{s}$, or $f_{sample} = 1\text{MHz}$

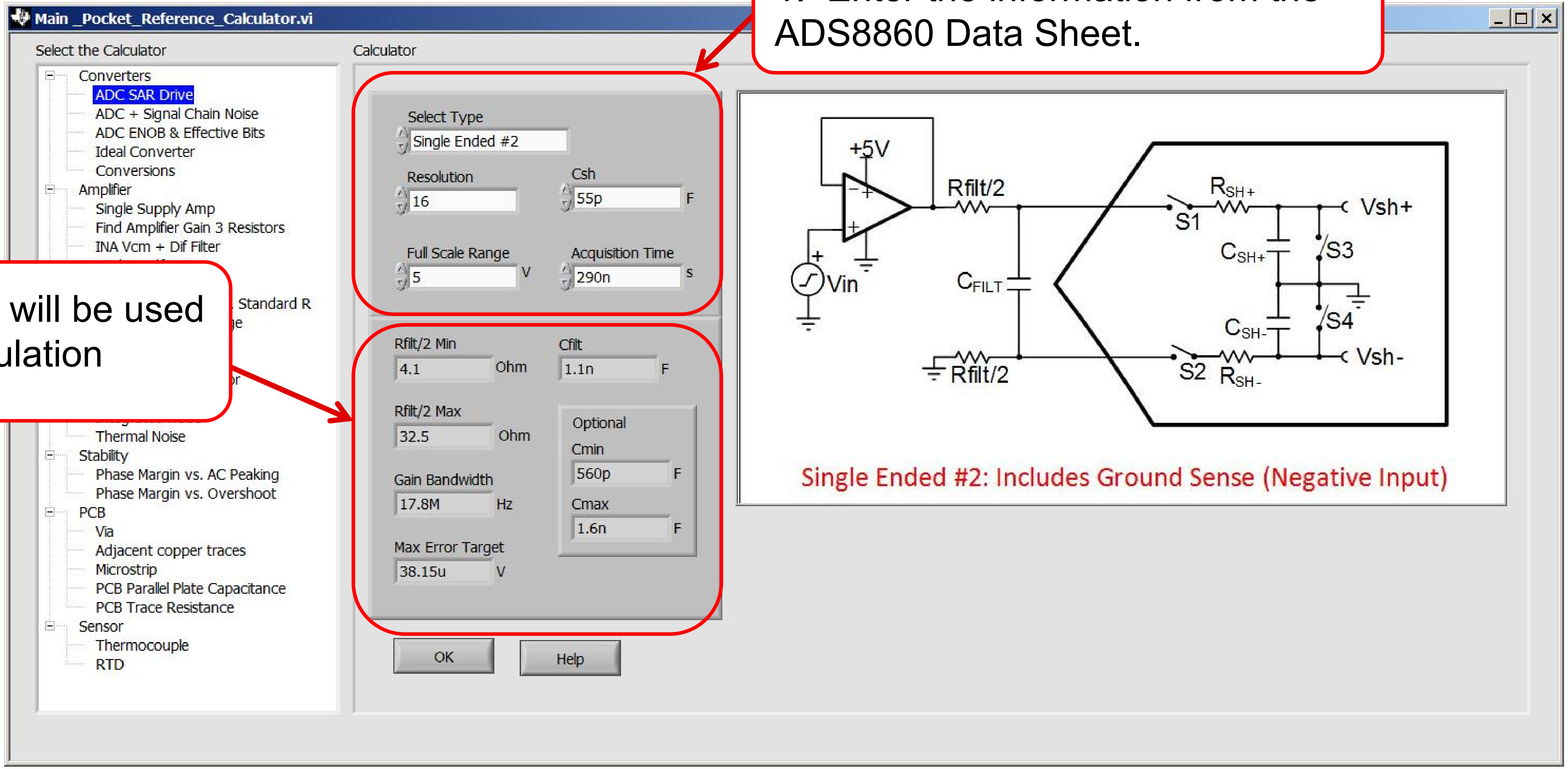
For cases where you aren't running at maximum throughput (e.g. 500kHz)

$t_{acq} = 1/f_{sample} - t_{conv\text{-}max} = (1/500\text{kHz}) - 710\text{ns} = 1290\text{ns}$

Run the "ADC SAR Drive" tool: ADS8860 Example

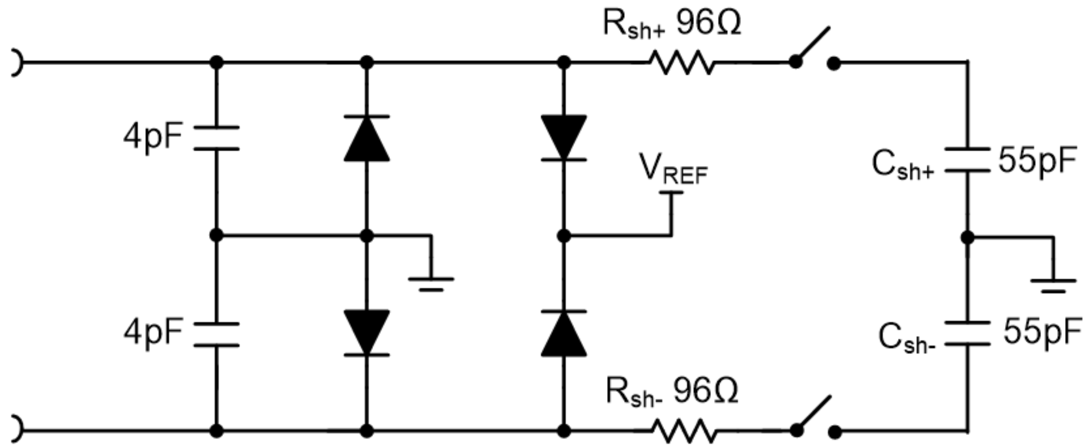
1. Enter the information from the ADS8860 Data Sheet.

2. Results will be used in the simulation

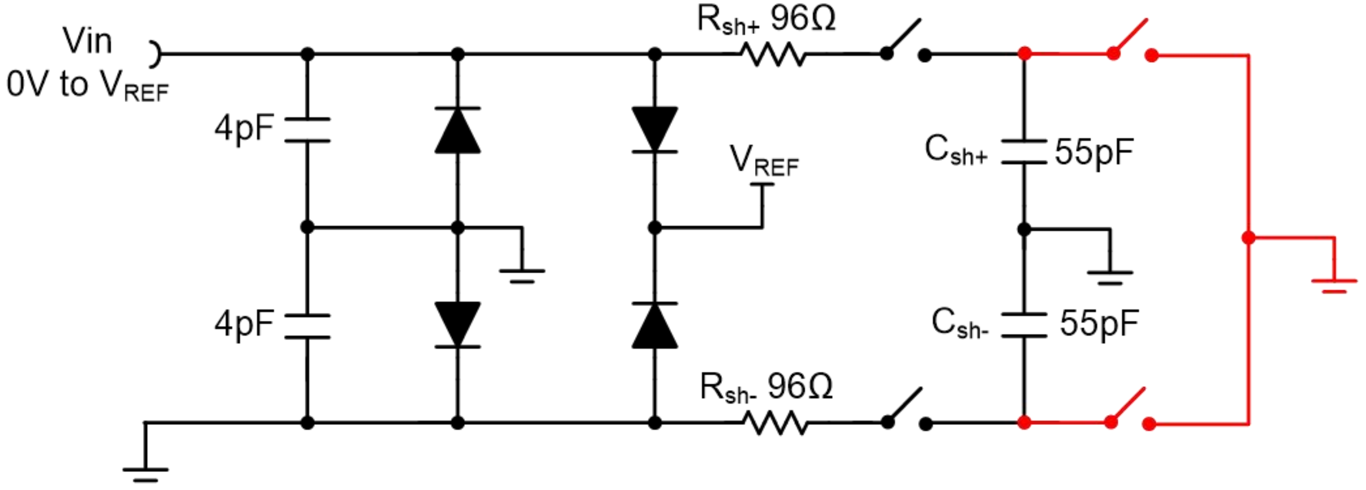


Simplifying the input model

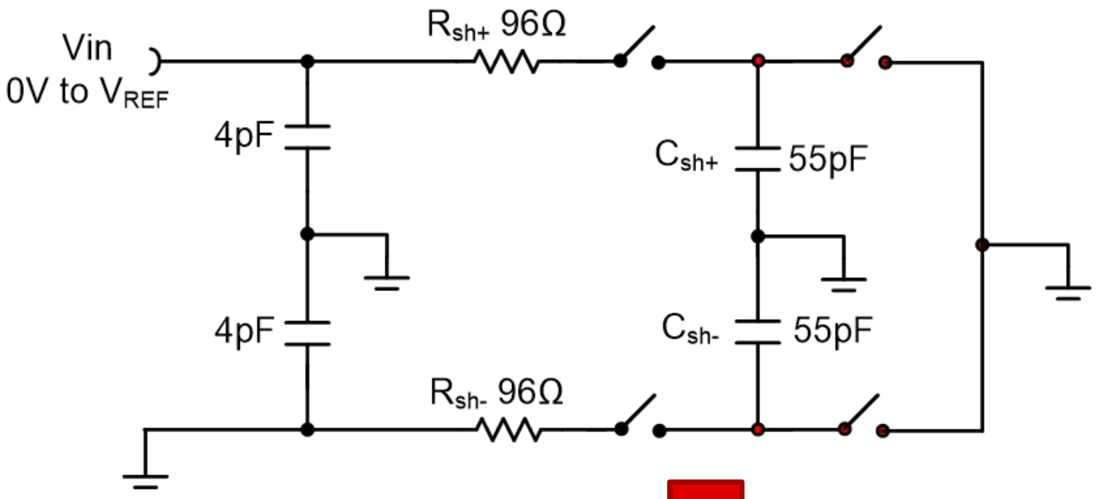
1) Input Circuit from the data sheet



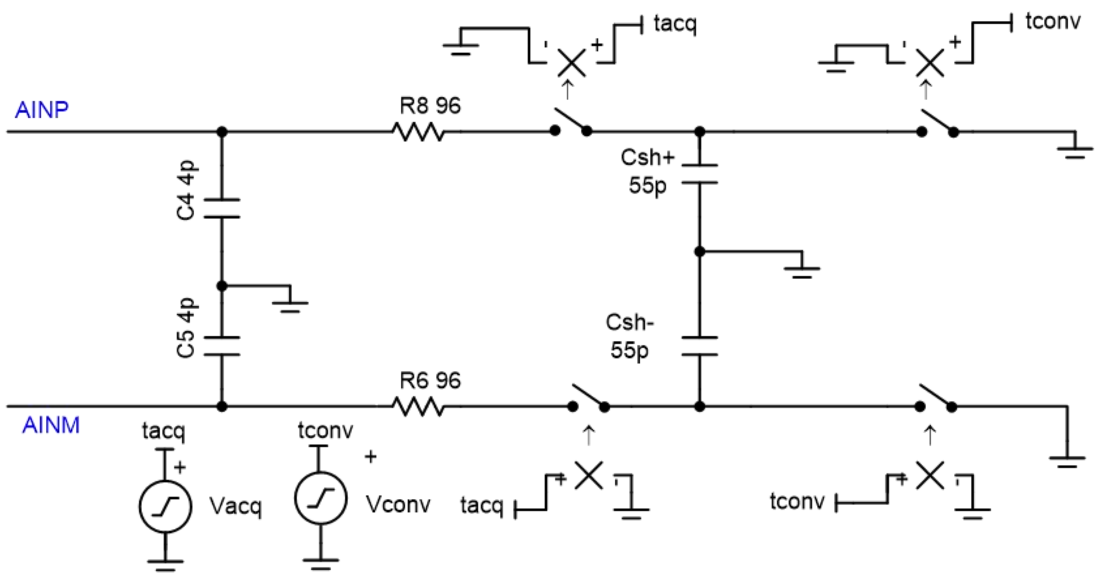
2) Add the sample and hold reset circuit



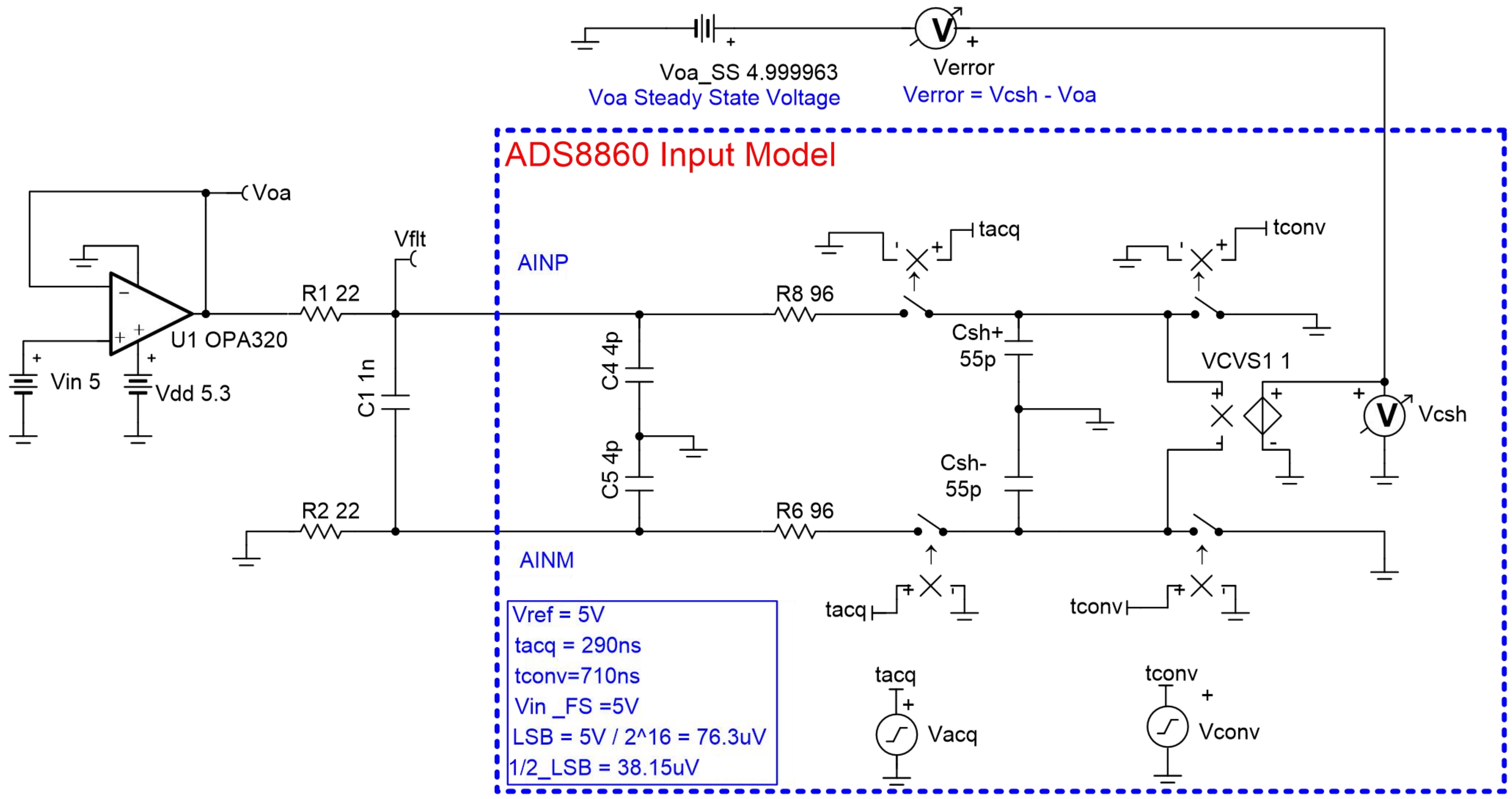
3) Diodes are reverse bias



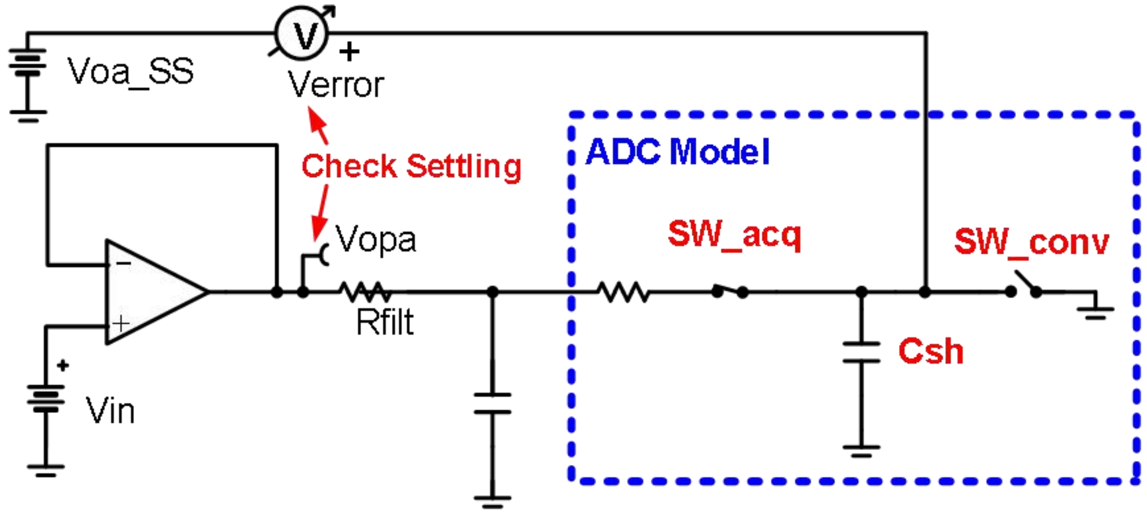
4) TINA Spice Model



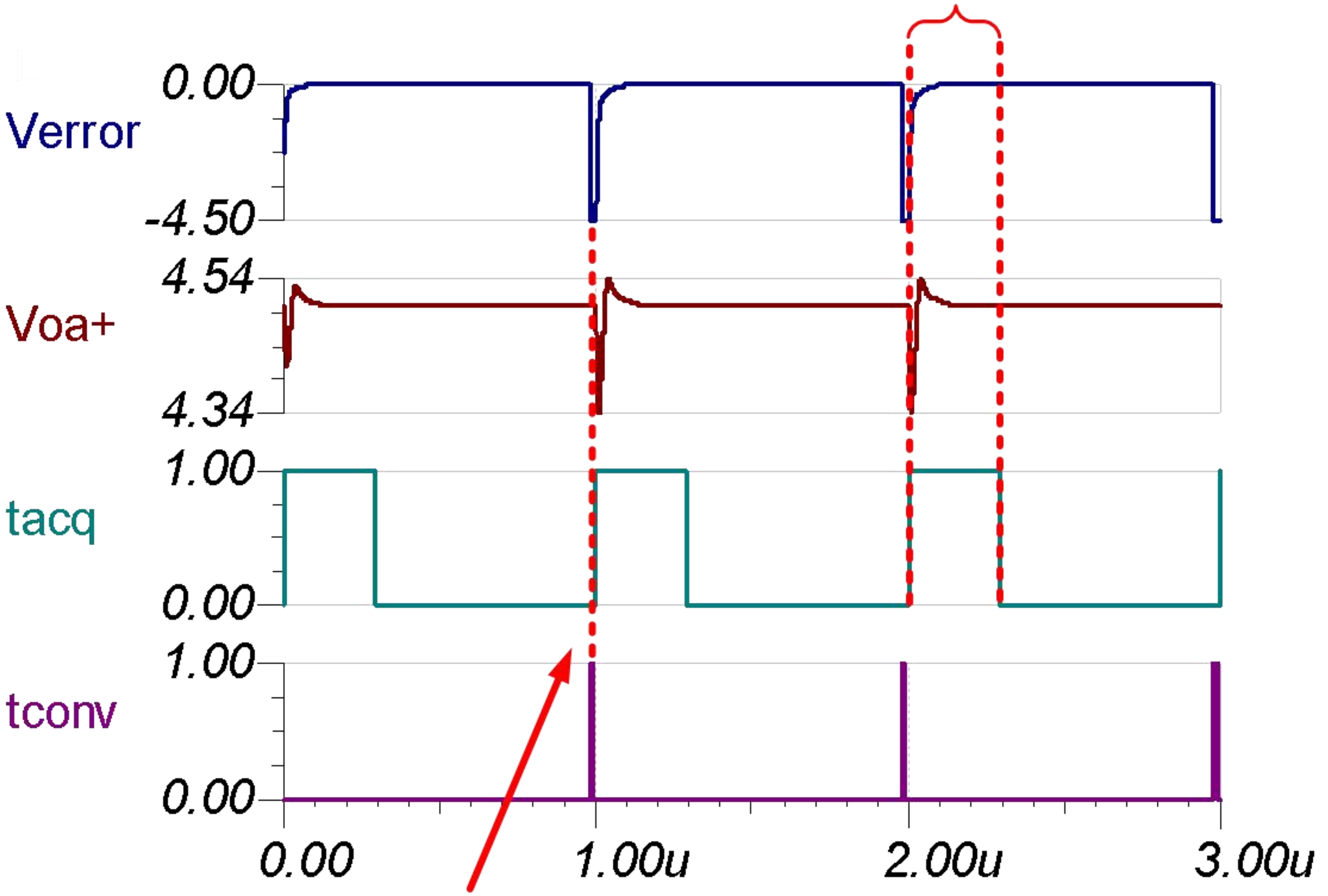
TINA SPICE Equivalent Model



Key Result: Error Signal



When tacq = 1V SW_acq is closed
Verror and Vopa must settle in this window



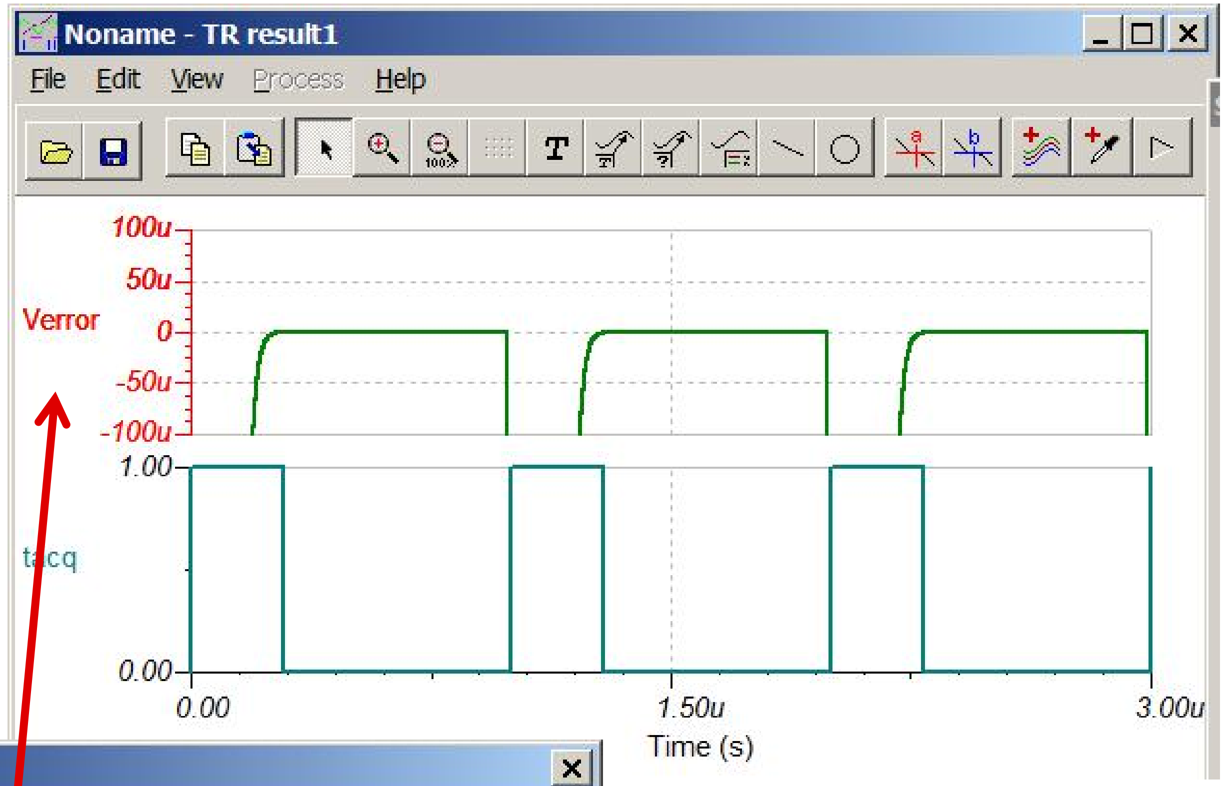
When tconv = 1V SW_conv is closed
This resets the internal S &H Capacitor Csh

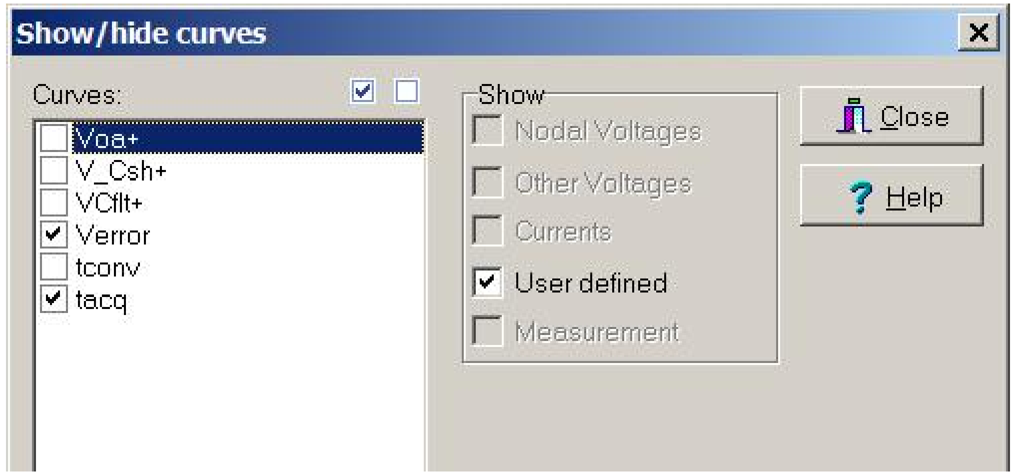
Zoom in on Error Signal

$N = 16$ Number of bits

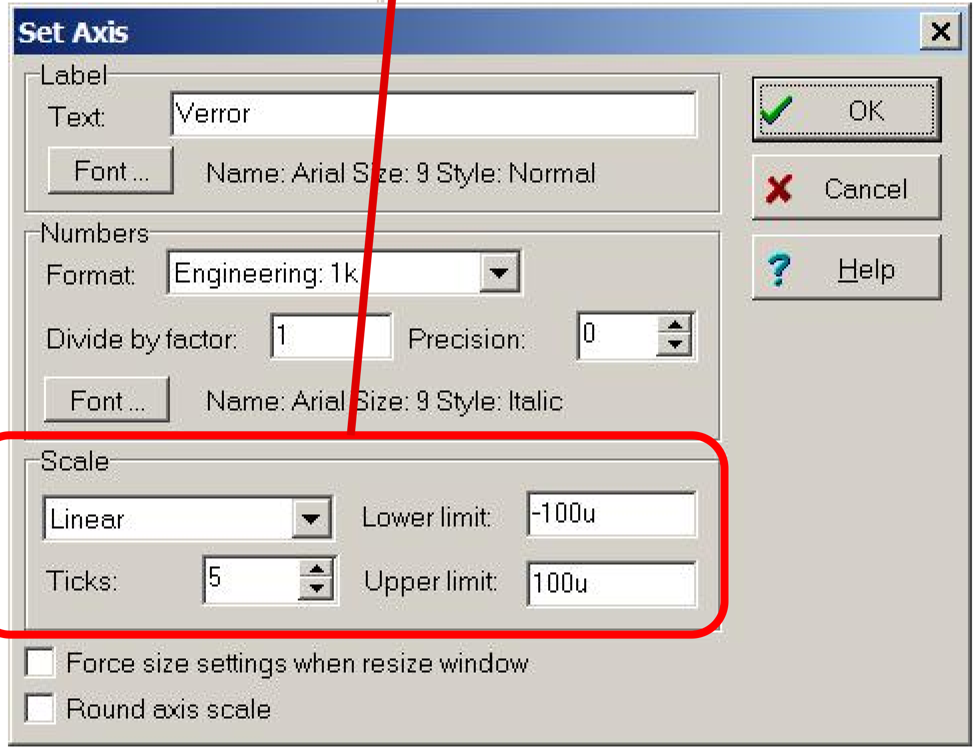
$LSB = \frac{FSR}{2^N} = \frac{5.0V}{2^{16}} = 76.3\mu V$ Resolution

$0.5 \cdot LSB = 38.1\mu V$ Target Error



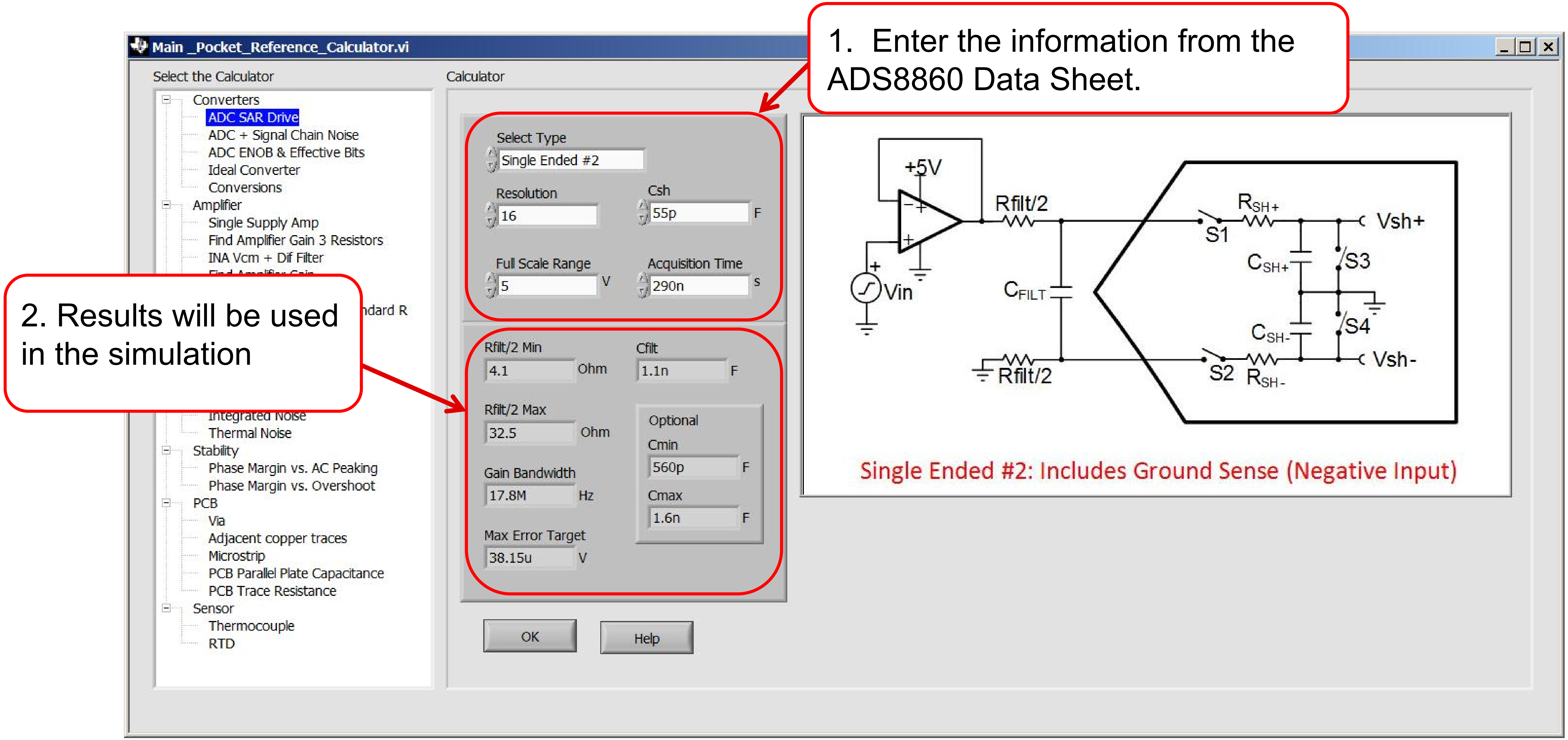


Use “view>show / hide curves” to focus on most important curves.

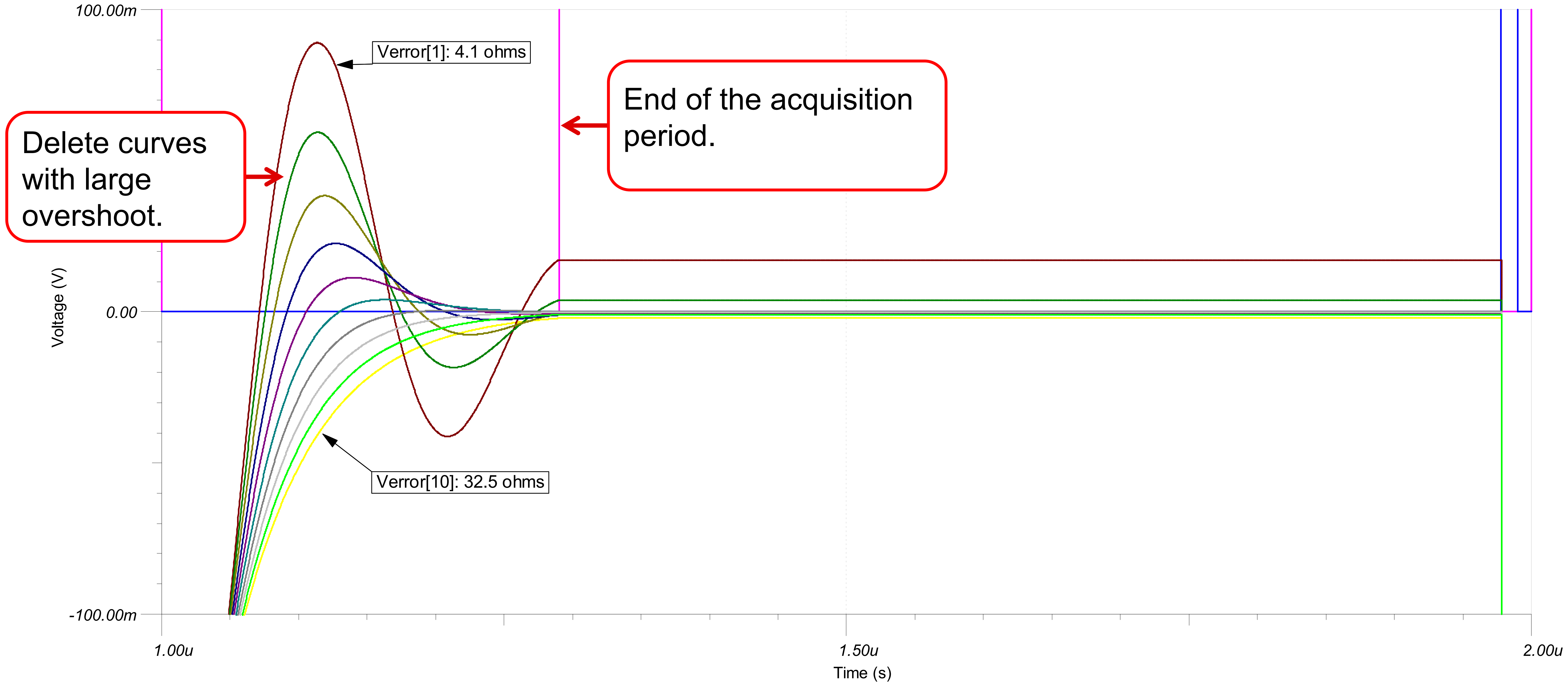


Click on axis and adjust the scale relative to LSB resolution.

Remember: ADS8860 example calculator results

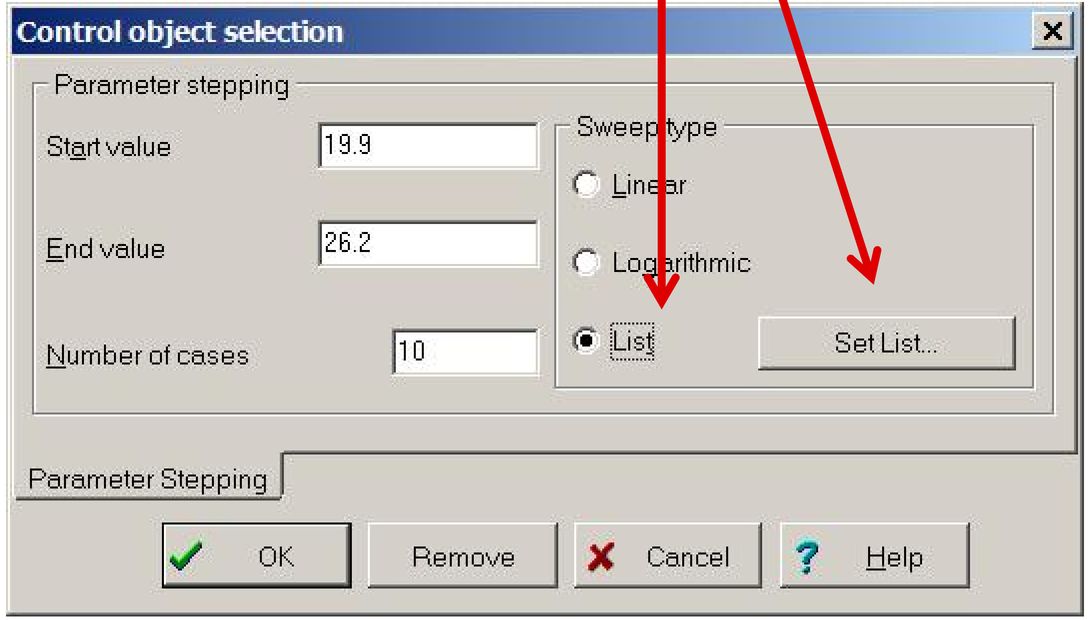


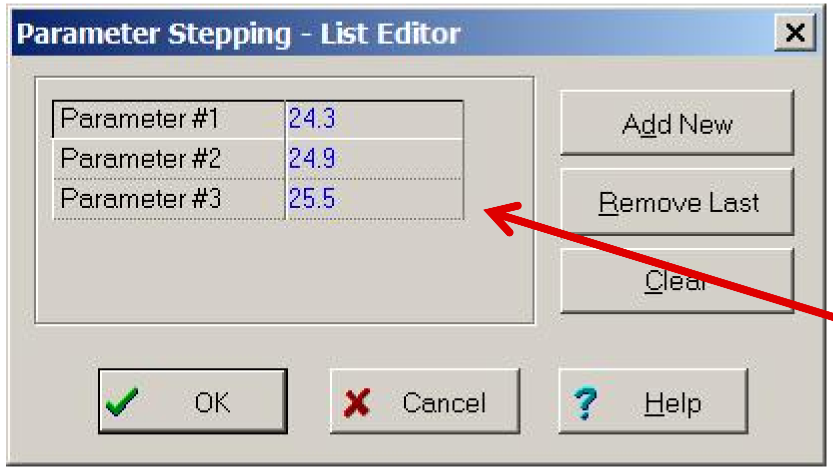
Error for R = 4.1 ohms…32.5 ohms



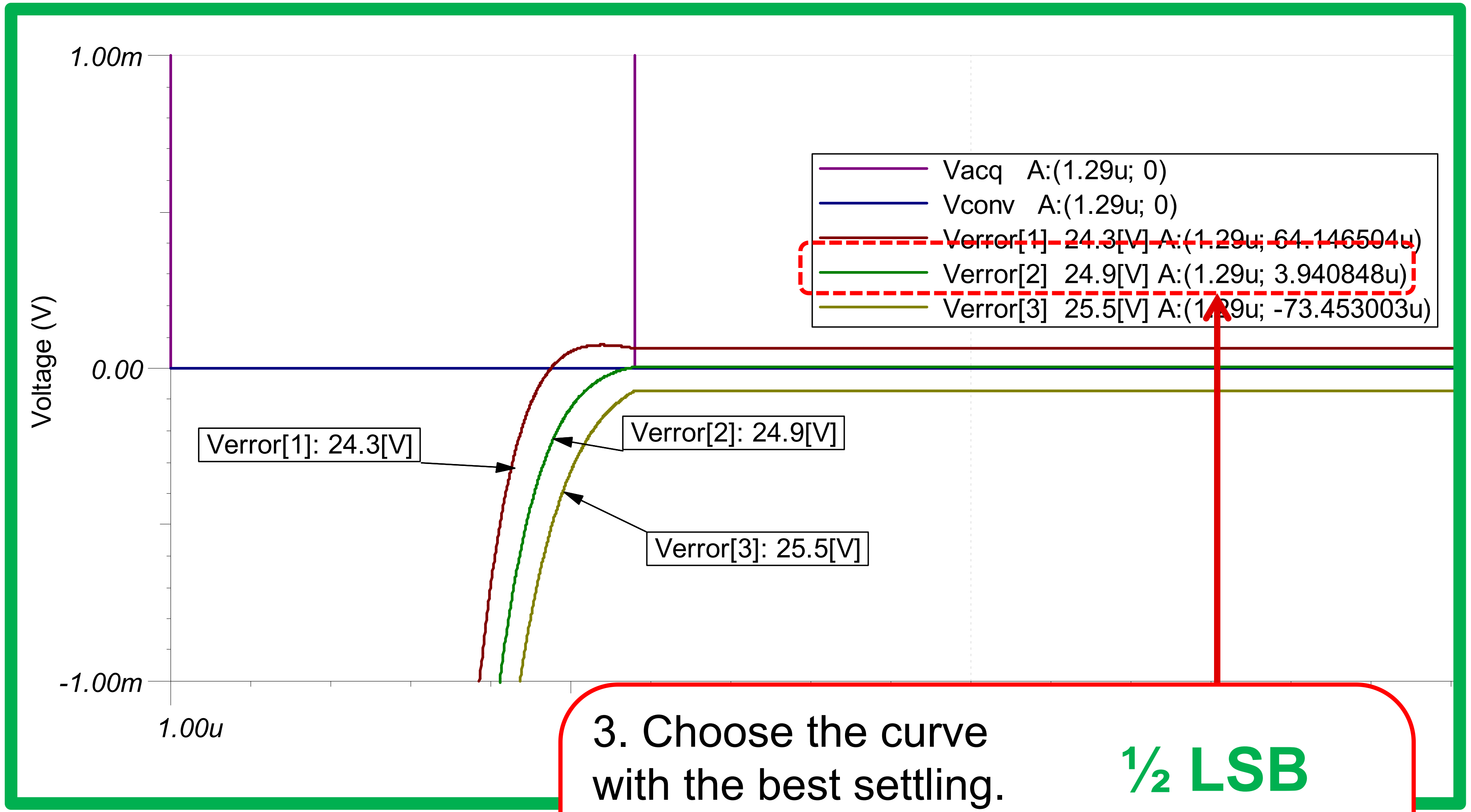
Final Run: Use Standard Values

1. Use the "List" sweep type





2. Enter standard resistor values using the results of the previous sweep (i.e. 24.1 to 25.5)

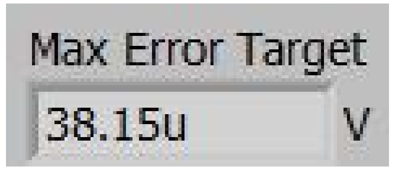


3. Choose the curve with the best settling. Check to see if the error target from the calculator is met.

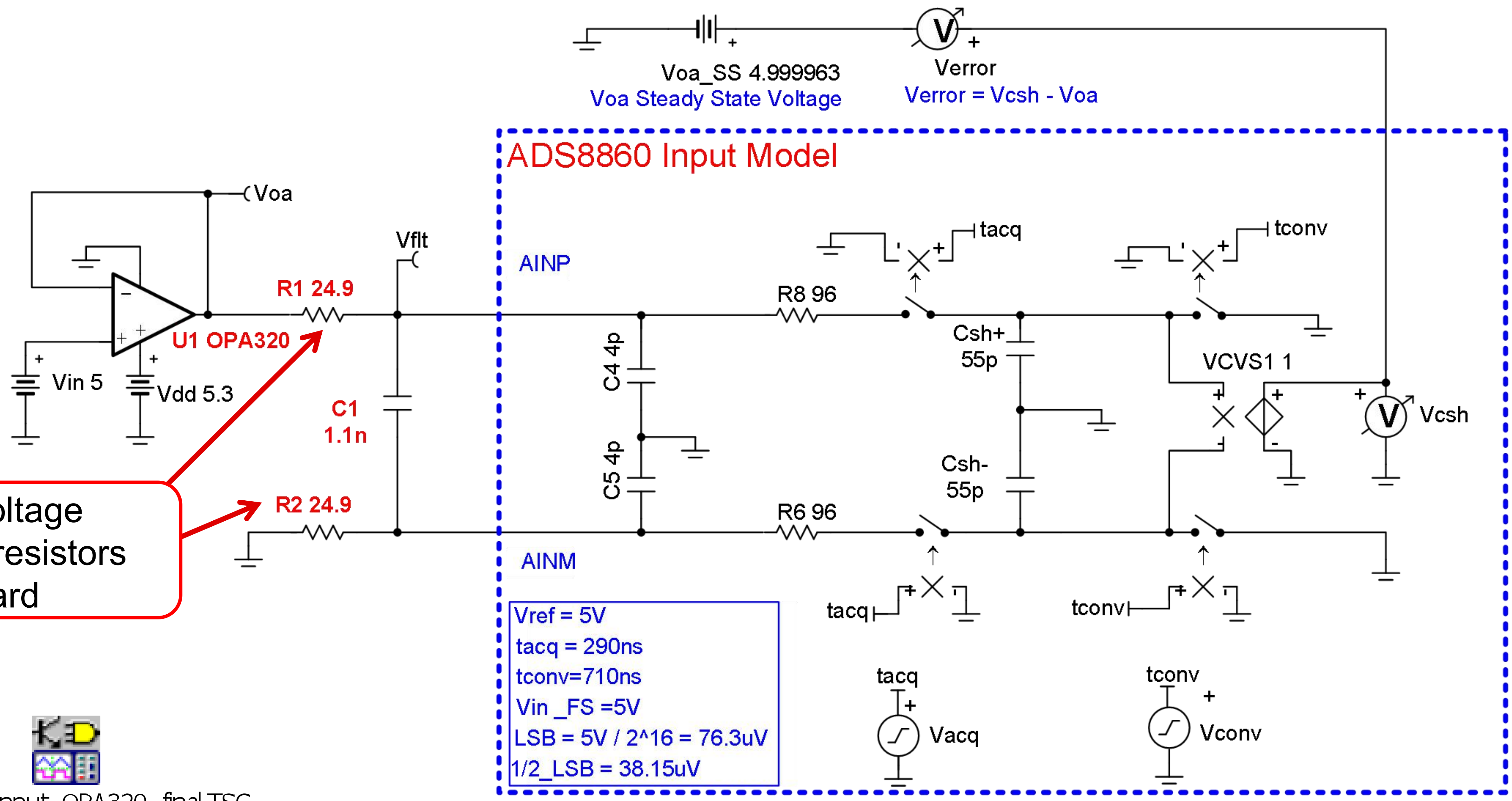
Yes! 3.9uV << 38.15uV

For R_{filt} = 24.9 Ω

½ LSB



Final Circuit



Replace voltage controlled resistors with standard resistors

ADS8860_Input_OPA320 -final.TSC

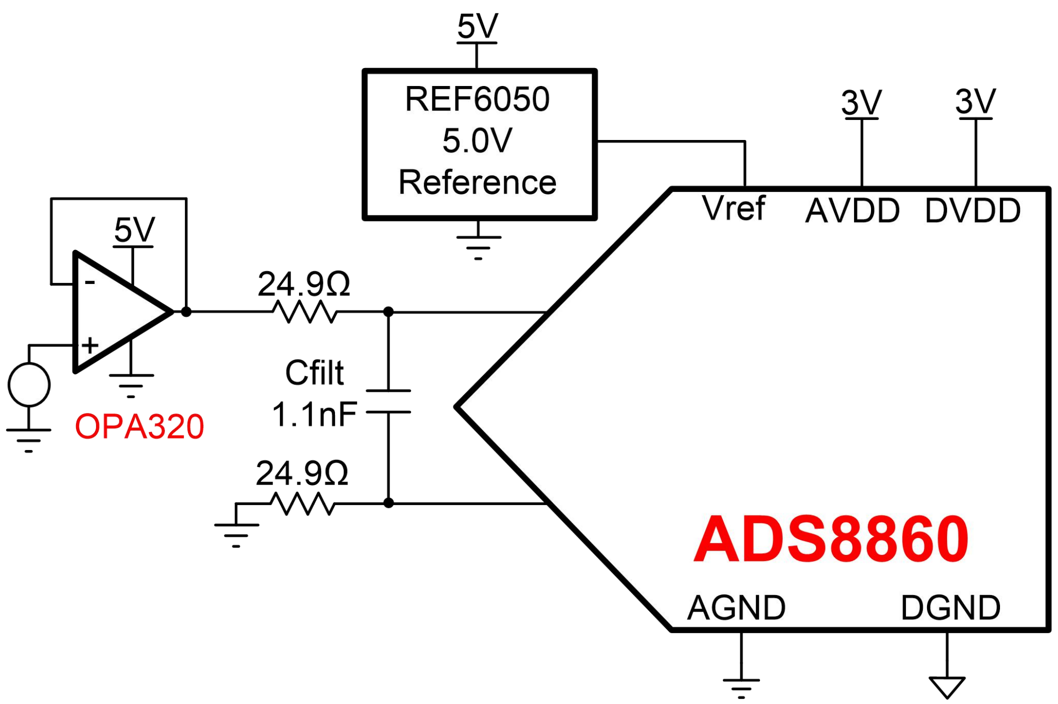
Demo – Good RC vs Bad RC Filter

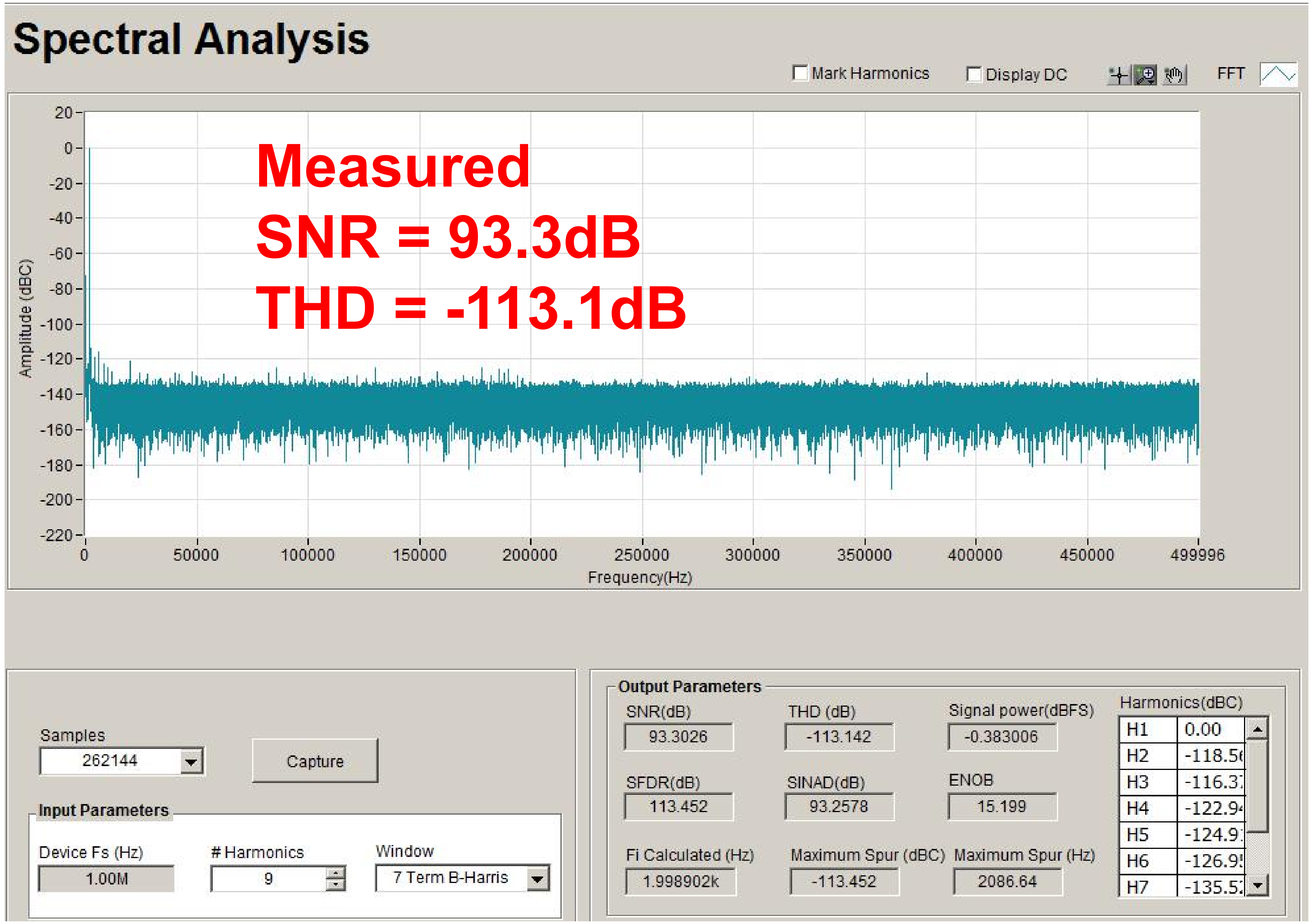
Measured results for example circuit

ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD (1kHz)		-108		dB

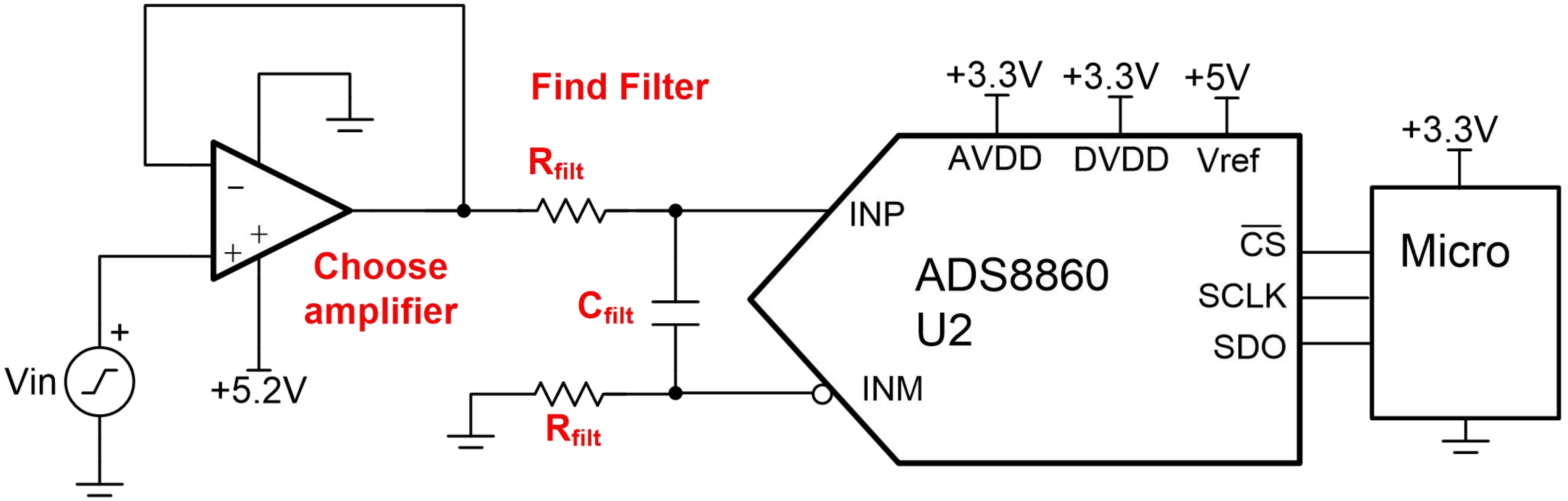
Circuit from TINA





SAR ADC Driver RC Optimization Experiment

Find amplifier and RC circuit



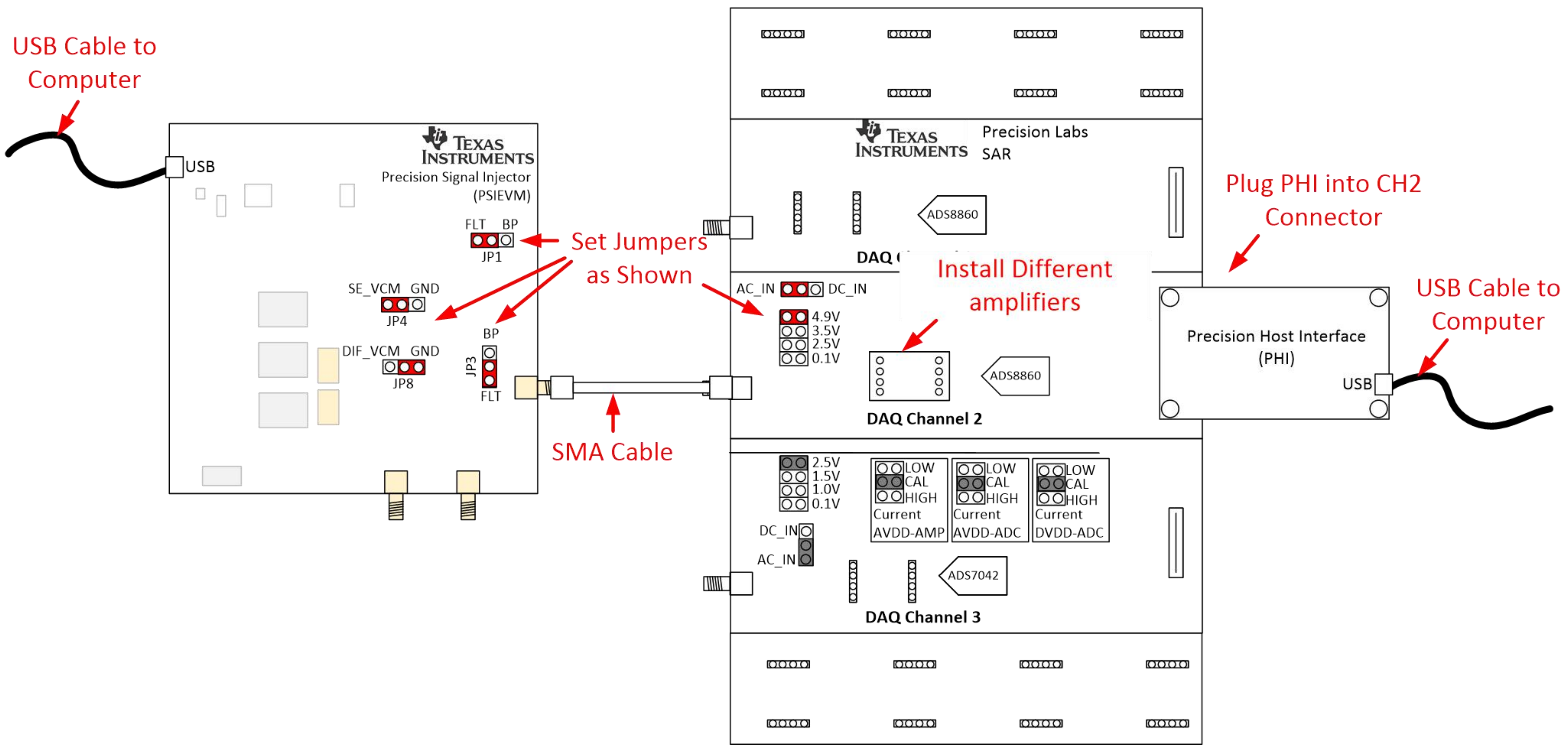
Amplifier:

- 5V, Rail-to-Rail I/O with Zero Crossover Distortion Required
- Find bandwidth using Analog Engineer's Calculator
- Use parametric search to find device.
- Verify model Open Loop Gain and Open Loop Output Impedance

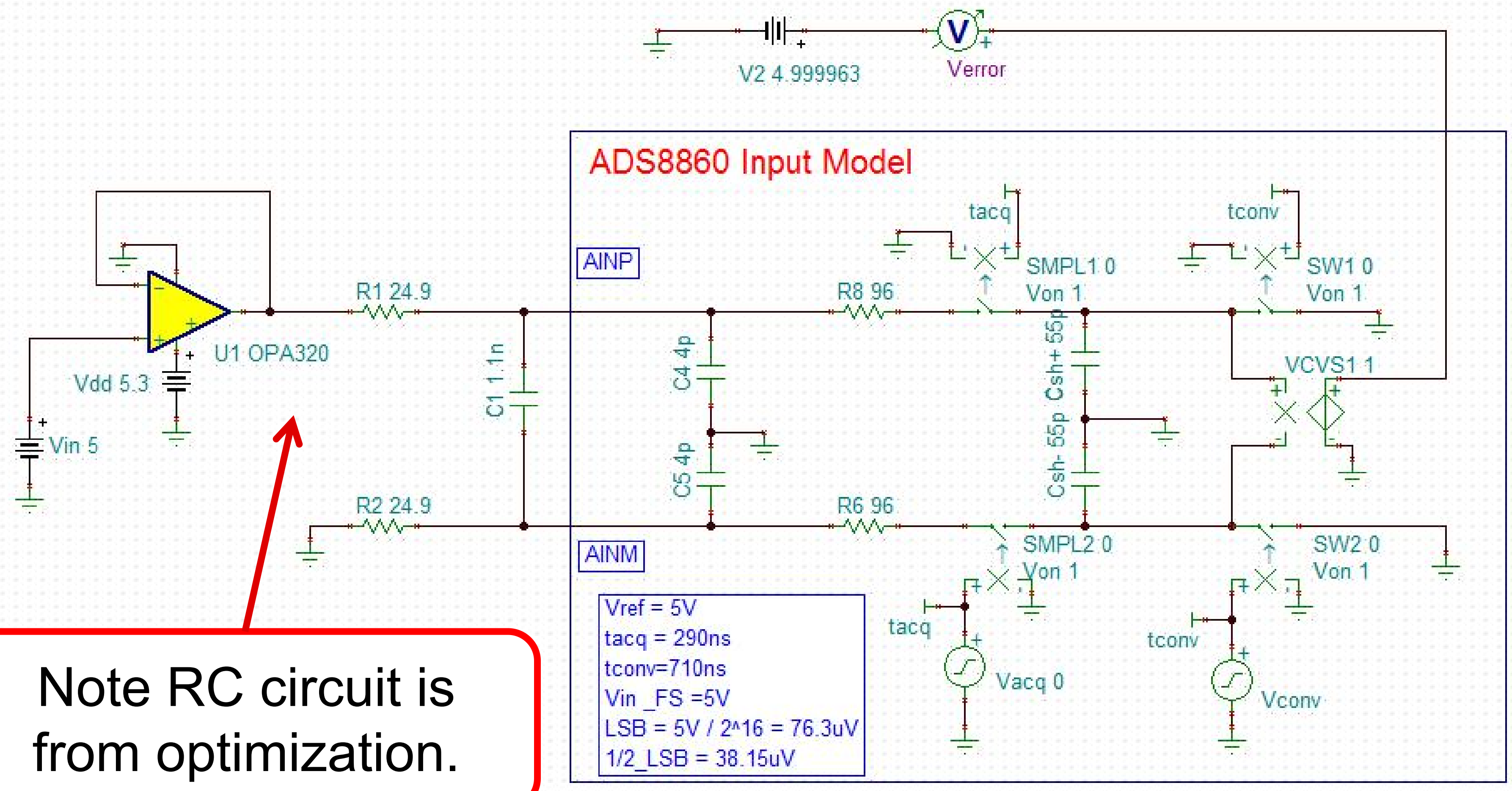
RC Charge Bucket Circuit:

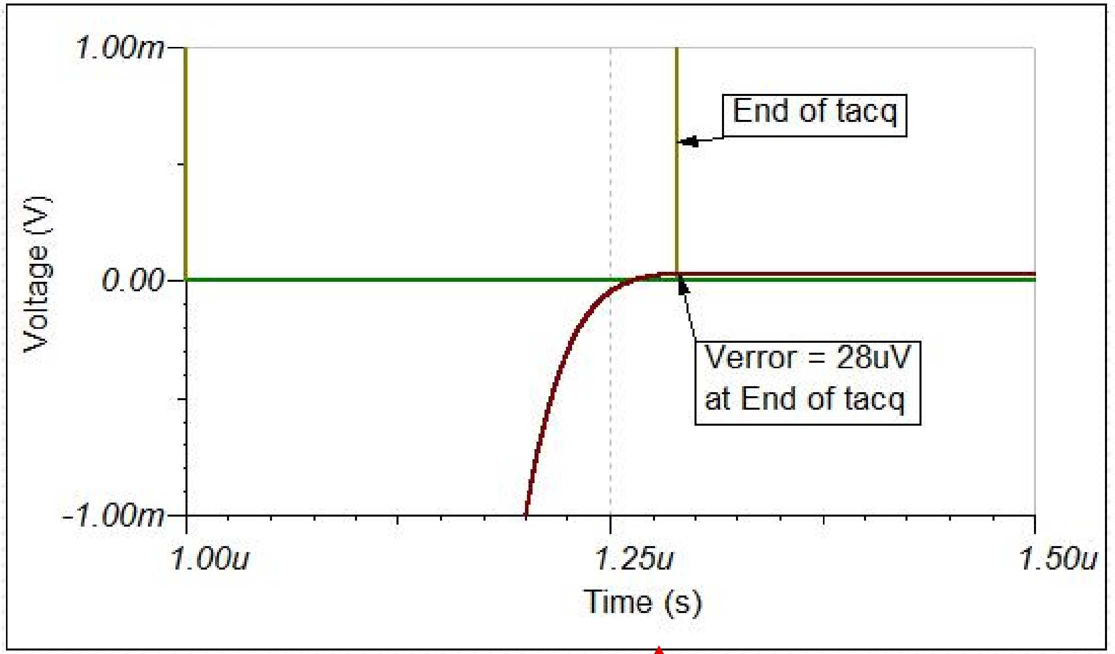
- Use Analog Engineer's Calculator for initial values
- Use TINA Simulation to Optimize

4a: Connect the hardware



1: OPA320_Good Filter1





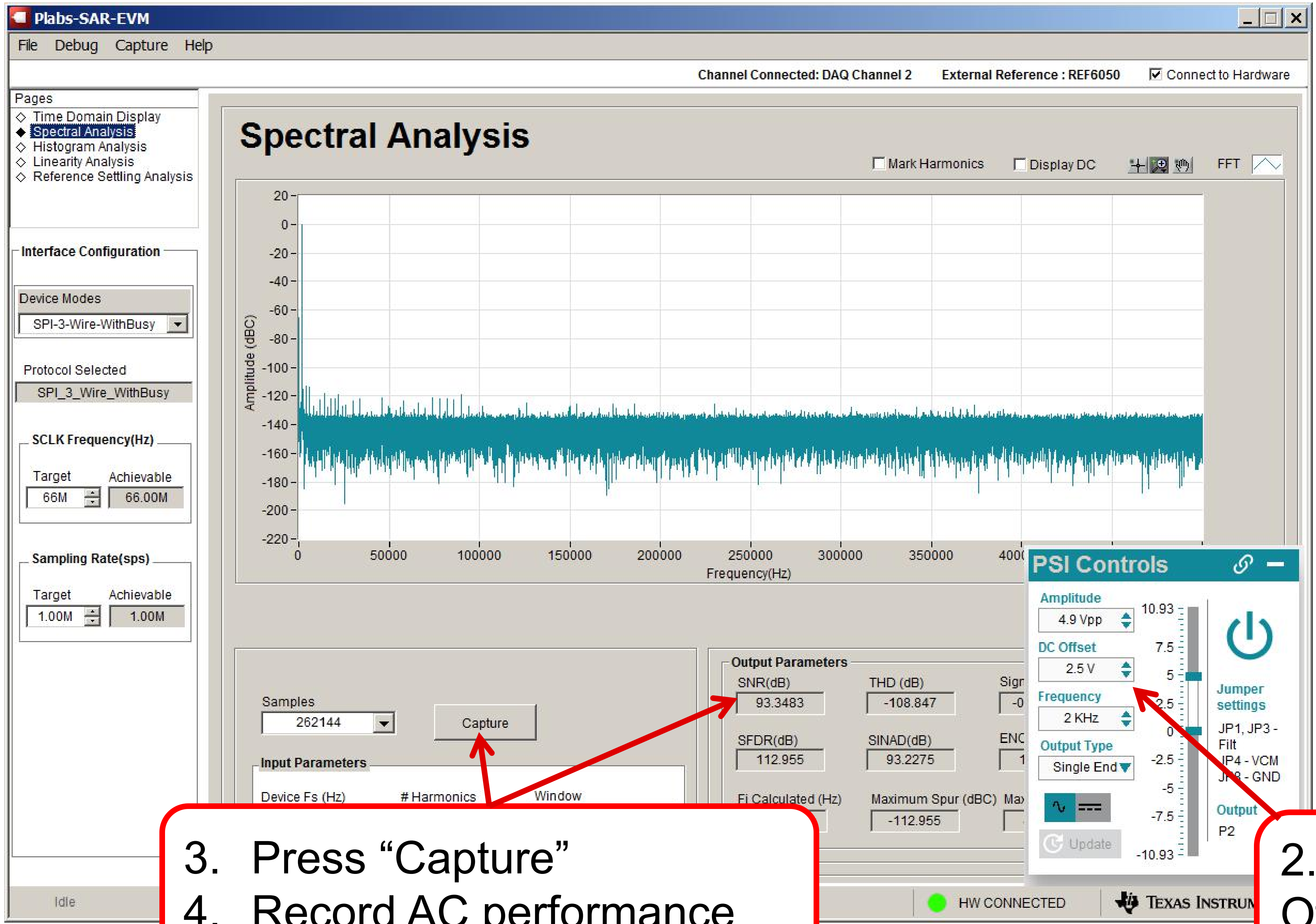
Note RC circuit is from optimization.

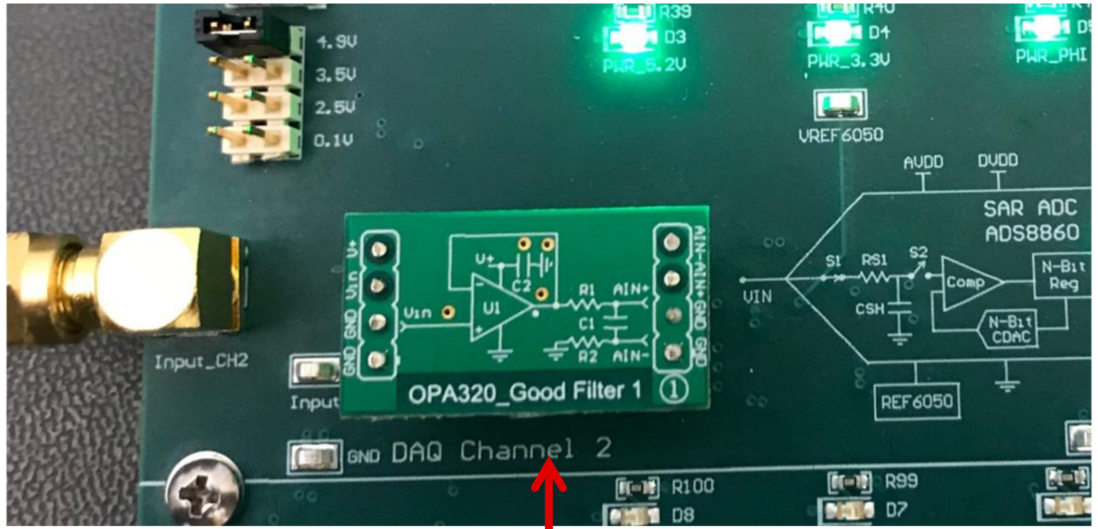
Error Target = 38µV
Simulate Error = 28µV

ADS8860_OPA320 - good filter.TSC

1: OPA320_Good Filter1

	SNR (dB)	THD (dB)
ADS8860 Spec.	93	-108
Good Filter 1	93.3	-108.8



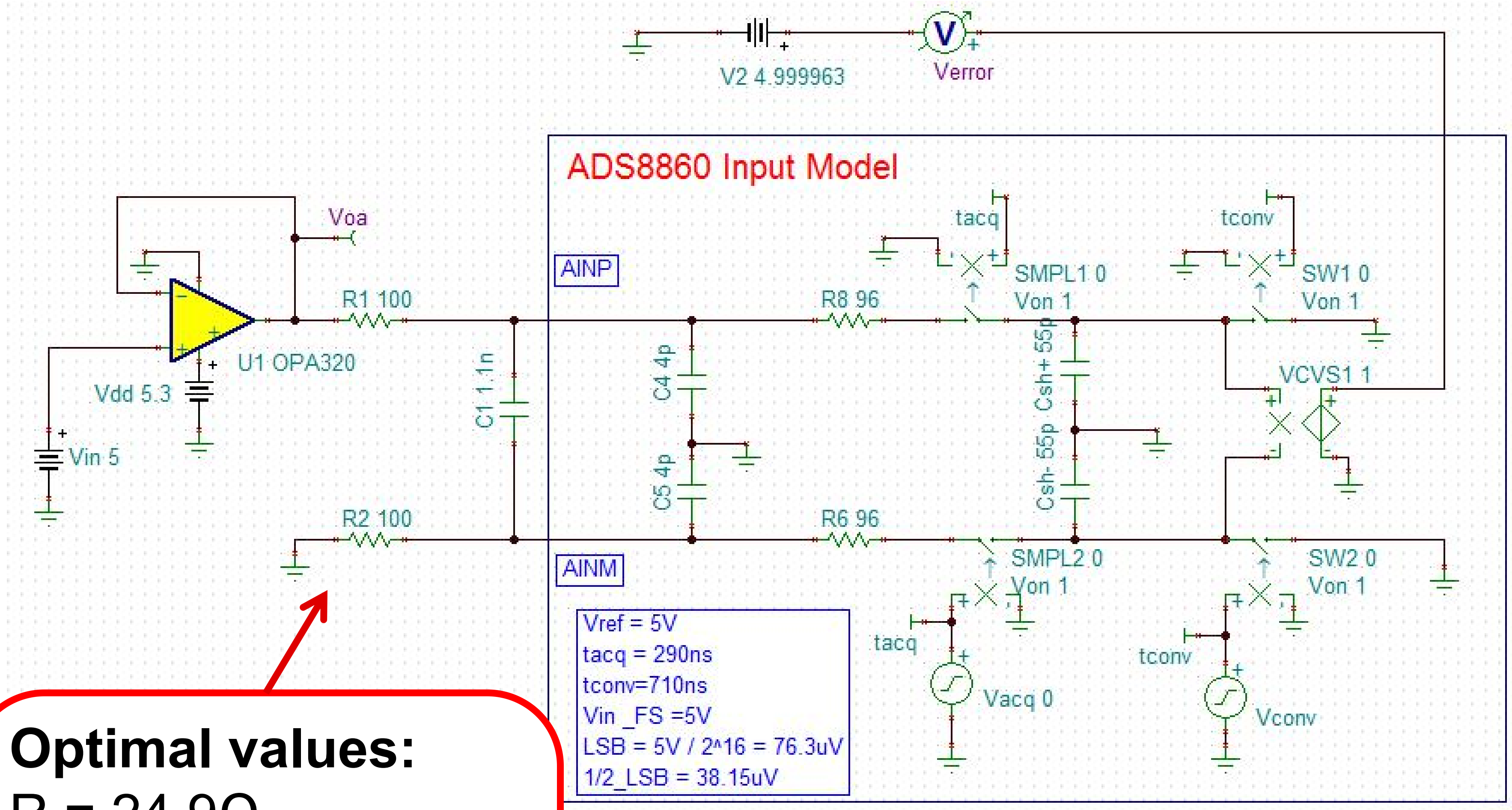


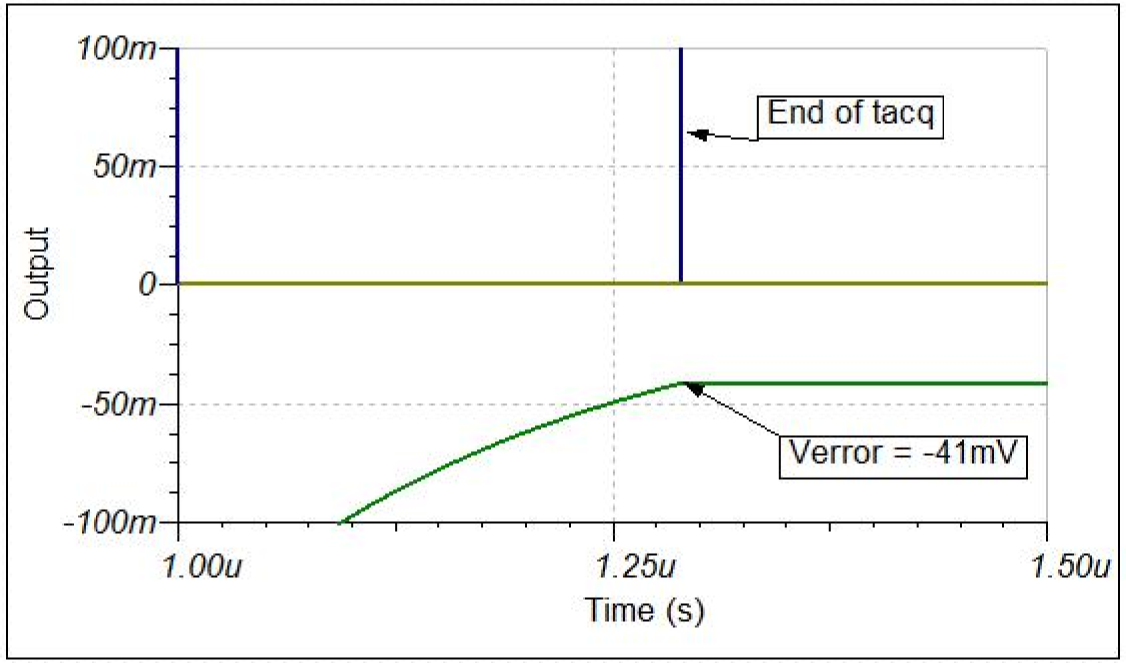
1. Install OPA320_Good filter 1 coupon card in socket.

2. Amplitude = 4.9V
Offset = 2.5V
Frequency = 2kHz

3. Press "Capture"
4. Record AC performance

2: OPA320 Bad Filter





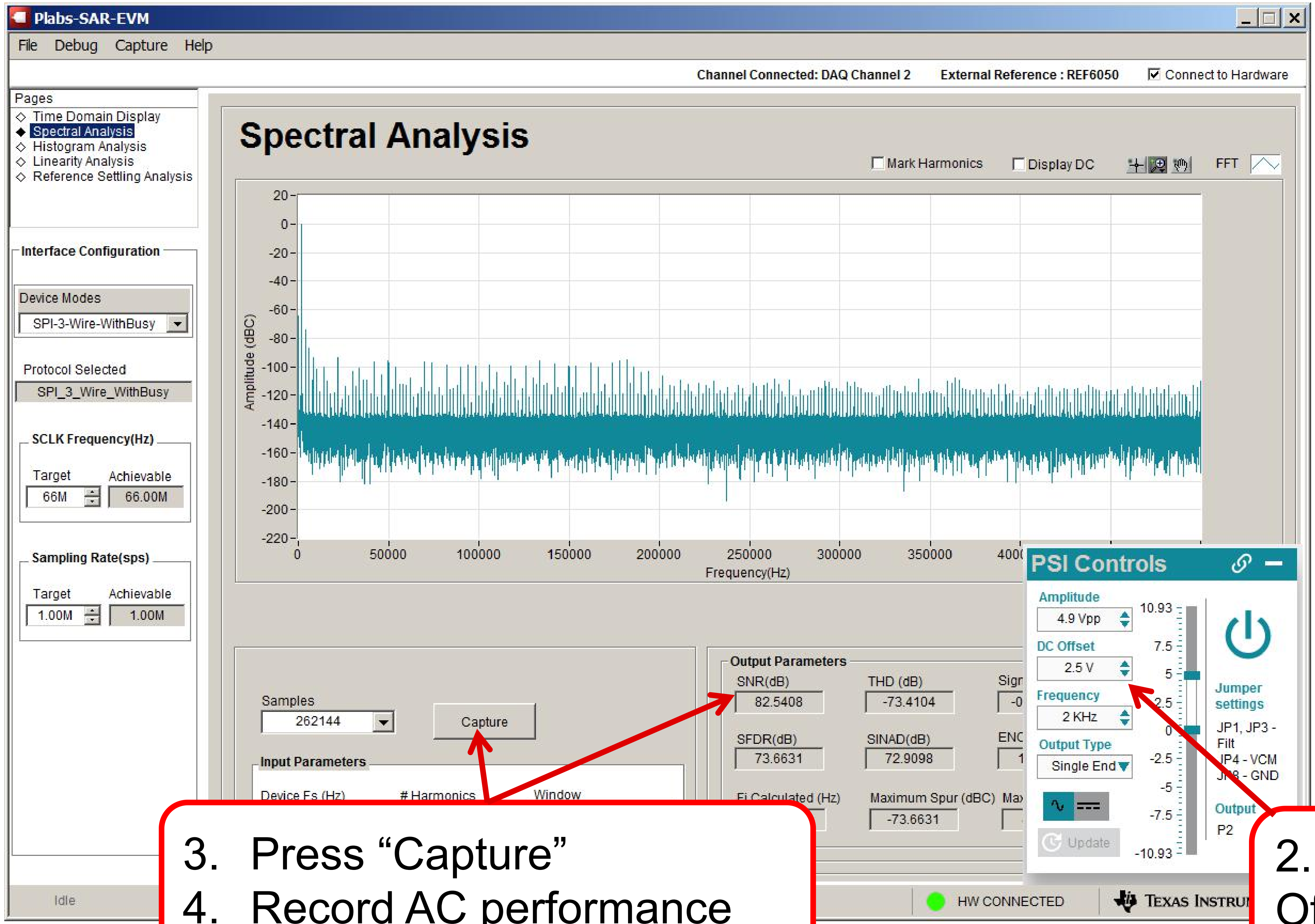
ADS8860_OPA320 - bad filter.TSC

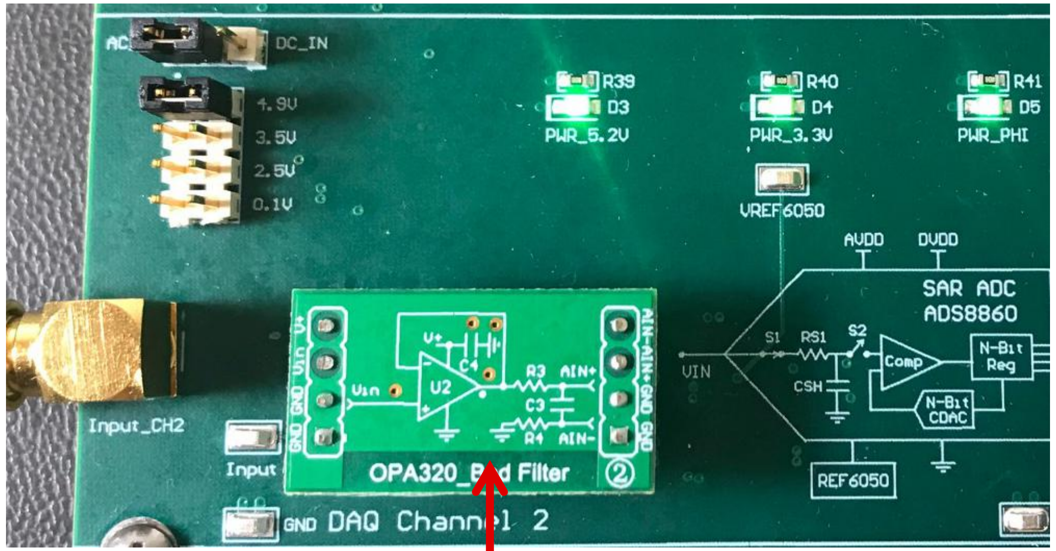
Optimal values:
R = 24.9Ω
C = 1.1nF
Bad Filter Values:
R = 100Ω
C = 1.1nF

Error Target = 38µV
Simulate Error = -41mV

2: OPA320 Bad Filter

	SNR (dB)	THD (dB)
ADS8860	93	-108
Bad Filter	82.5	-73.4





1. Install OPA320_Bad Filter coupon card in socket.

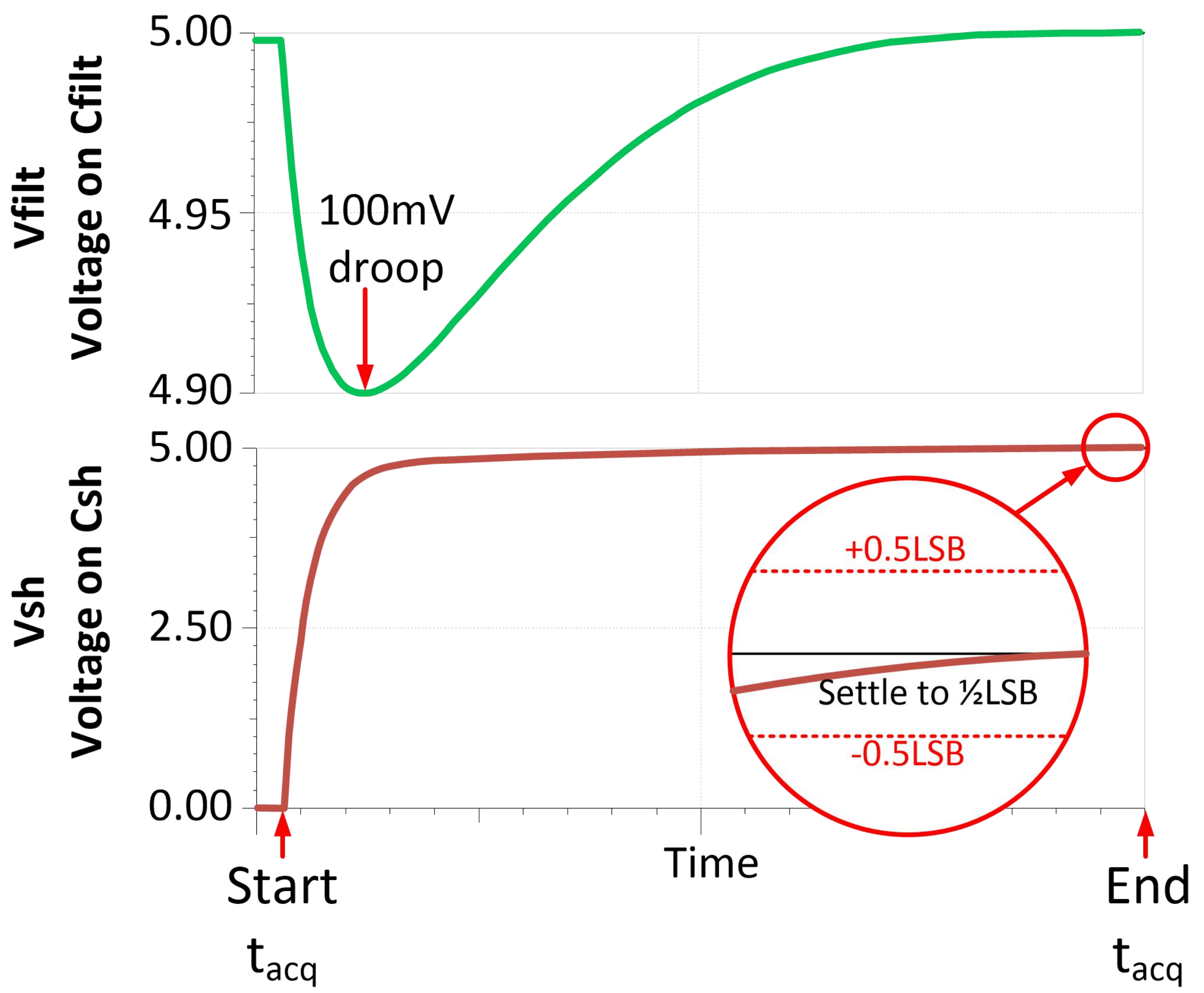
2. Amplitude = 4.9V
Offset = 2.5V
Frequency = 2kHz

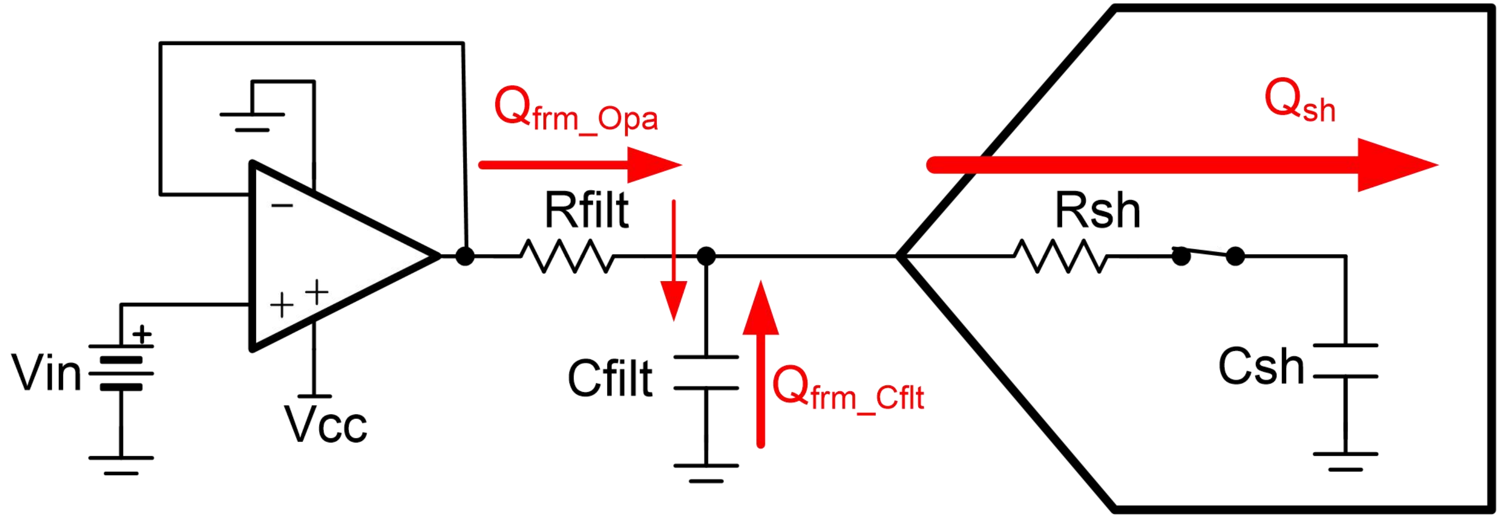
3. Press “Capture”
4. Record AC performance

How Driver Bandwidth Affecting ADC system

Speaker: Andrew Wang

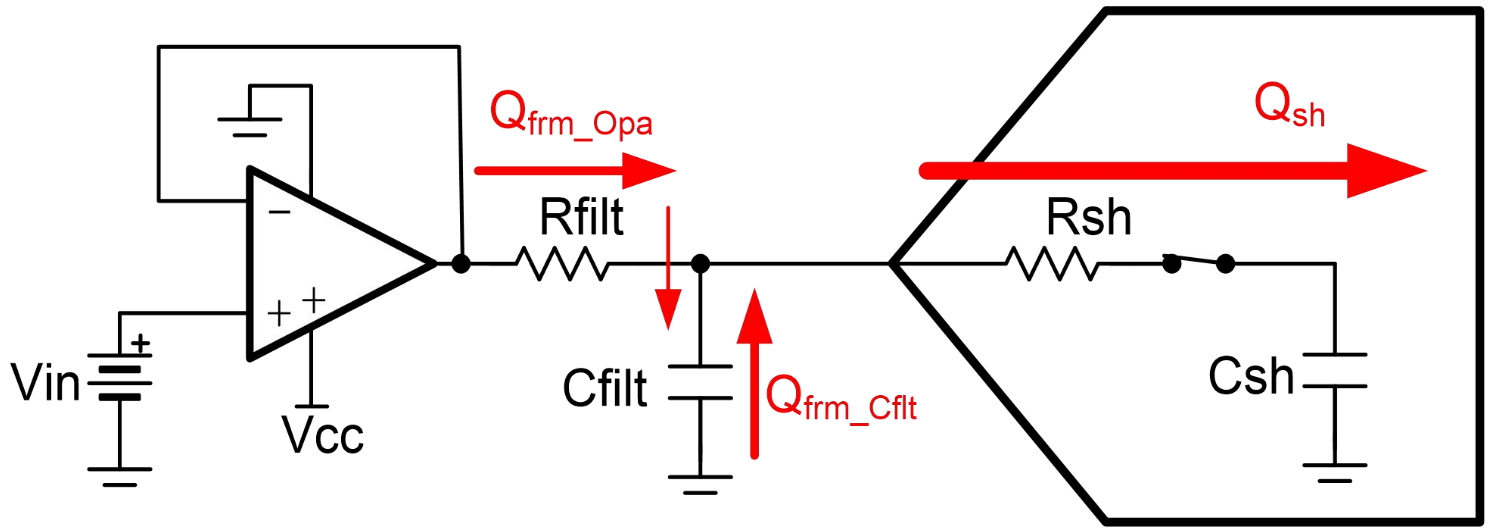
Concept behind the math





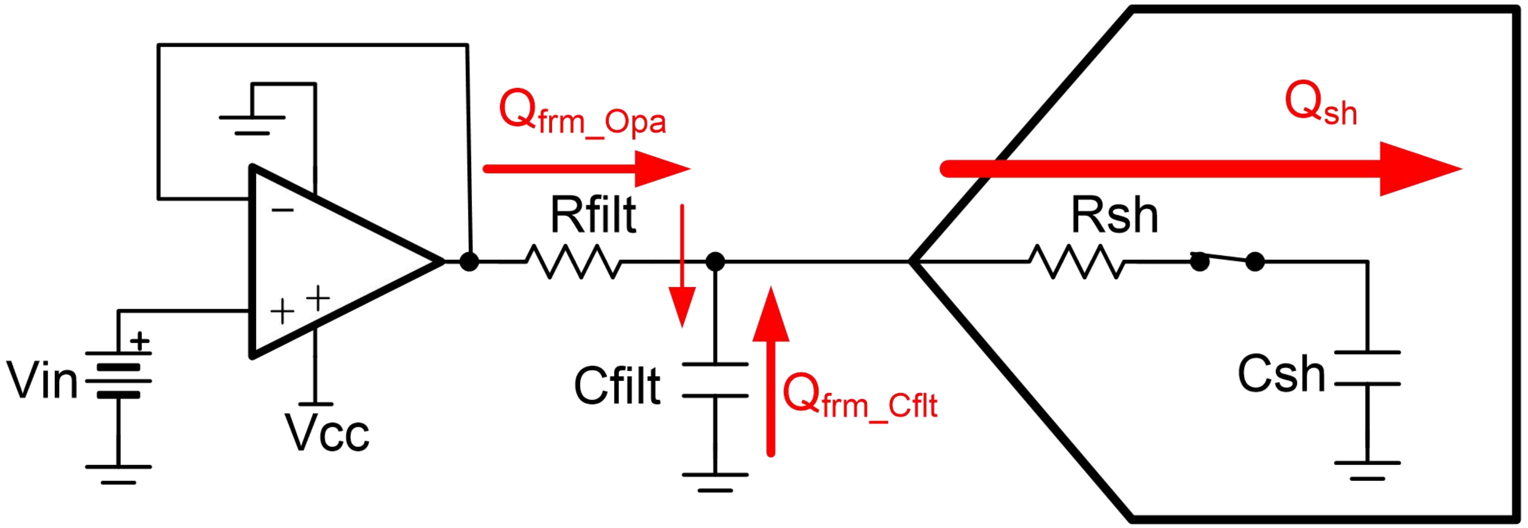
- Assumptions based on multiple designs
- Vin = Full Scale
- ½ of Q_{sh} is from C_{filt} & ½ from Op Amp
- 100mV Droop – small signal response
- Error target = 0.5·LSB
- Op amp approximated as second order system
- Op amp four times faster than filter

C_{filt} Selection



$Q_{sh} = V_{FSR} \cdot C_{sh}$	(1)	Total Charge in Csh and the end of acquisition period.
$Q_{sh} = Q_{frmOpa} + Q_{frmCfilt}$	(2)	Charge is from amplifier and filter capacitor
$\Delta Q_{Cfilt} = 0.5 \cdot Q_{sh}$	(3)	Half the sample and hold charge (Q_{sh}) is delivered from the filter. This results in a change in the charge on Cfilt.
$\Delta Q_{Cfilt} = 0.5 \cdot V_{FSR} \cdot C_{sh}$	(4)	From (1), and (3)
$\Delta Q_{Cfilt} = \Delta V_{filt} \cdot C_{filt}$	(5)	The change in charge on Cfilt will cause a droop in voltage. ΔV_{filt}
$C_{filt} = \left(\frac{0.5 \cdot V_{FSR}}{\Delta V_{filt}}\right) C_{sh}$	(6)	From (4), and (5). This is the general relationship for scaling Cfilt, given a droop in filter voltage (Vfilt)

C_{filt} Scaling Continued



$C_{filt} = \left(\frac{0.5 \cdot V_{FSR}}{\Delta V_{filt}}\right) C_{sh}$	(6)	From previous slide: This is the general relationship for scaling Cfilt, given a droop in filter voltage (Vfilt).
Assume $V_{FSR} = 4V,\ \Delta V_{filt} = 100mV$		
$\boldsymbol{C_{filt} = 20 \cdot C_{sh}}$	(7)	**Typical value for Cfilt**
$C_{filt} = 30 \cdot C_{sh}$	(8)	Maximum value for Cfilt
$C_{filt} = 10 \cdot C_{sh}$	(9)	Minimum value for Cfilt

Note 1: Experience shows that using the fixed factors of 20 yields good results.
Note 2: In rare cases, you may need to sweep Cfilt. Thus the factors of 10 and 30.

Time constant required for settling to error target

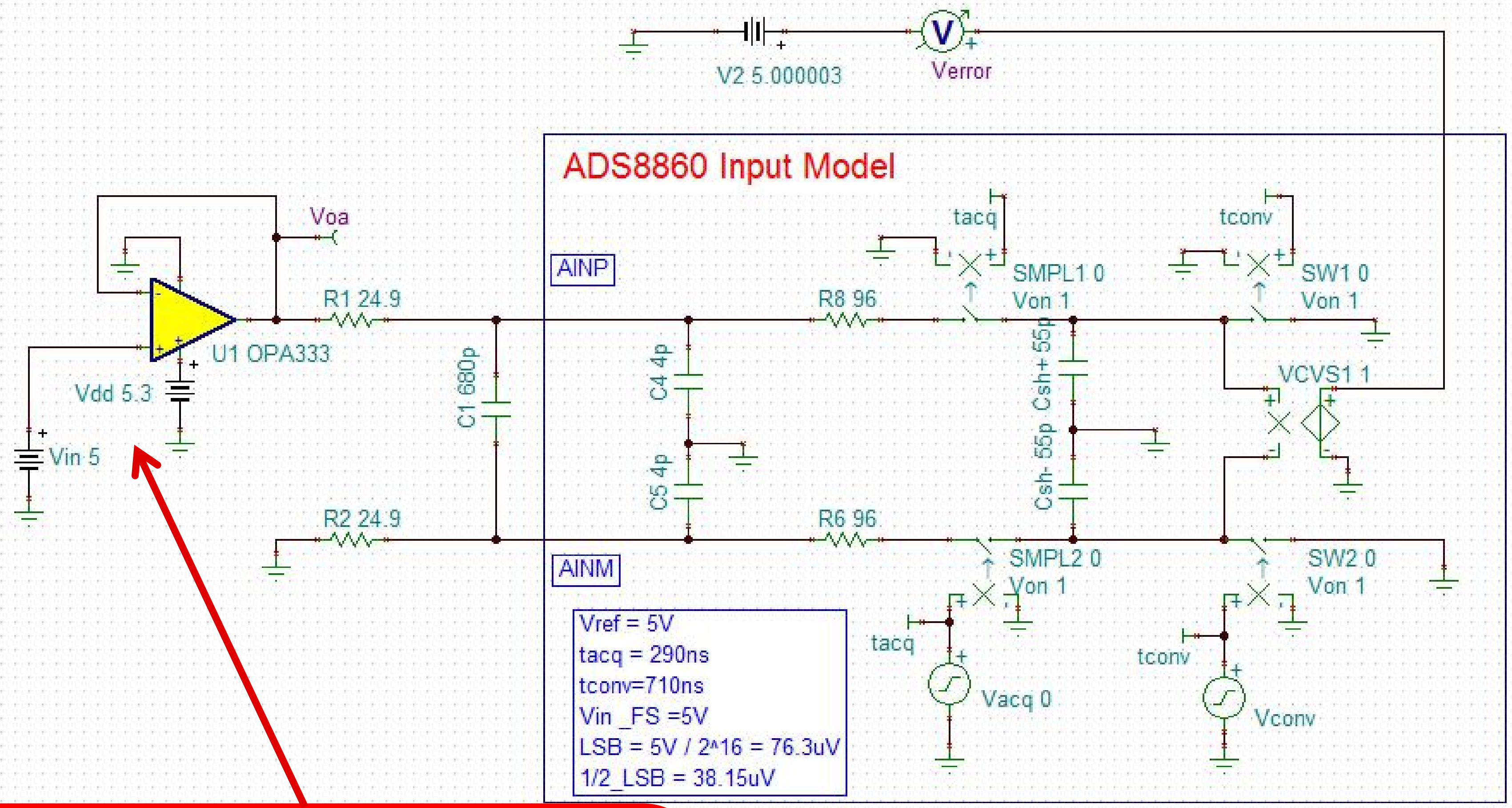
$V_{filt} = \left(V_{init} - V_{final}\right) \cdot e^{-t/\tau_c} + V_{final}$	(10)	This is the standard RC charge equation. τ_c = time constant for charging C_{sh}. V_{init} = initial voltage at start of t_{acq} V_{final} = final voltage for fully charged C_{filt}
$0.5 \cdot LSB = V_{final} - V_{filt}$	(11)	Error is less than ½ LSB
$V_{init} - V_{final} = 100mV$	(12)	Droop is 100mV
$0.5 \cdot LSB = (100mV) \cdot e^{-t/\tau_c}$	(13)	Substitute 11 and 12 into 10
$\tau_c = \dfrac{-t_{acq}}{\ln\left(\dfrac{0.5 \cdot LSB}{100mV}\right)}$	(14)	Solve (13) for τ_c Note: τ_c includes effects from Op Amp and C_{filt} The op amp is being modeled as a second order system (RC circuit)

Find Rfilt and Amplifier Bandwidth

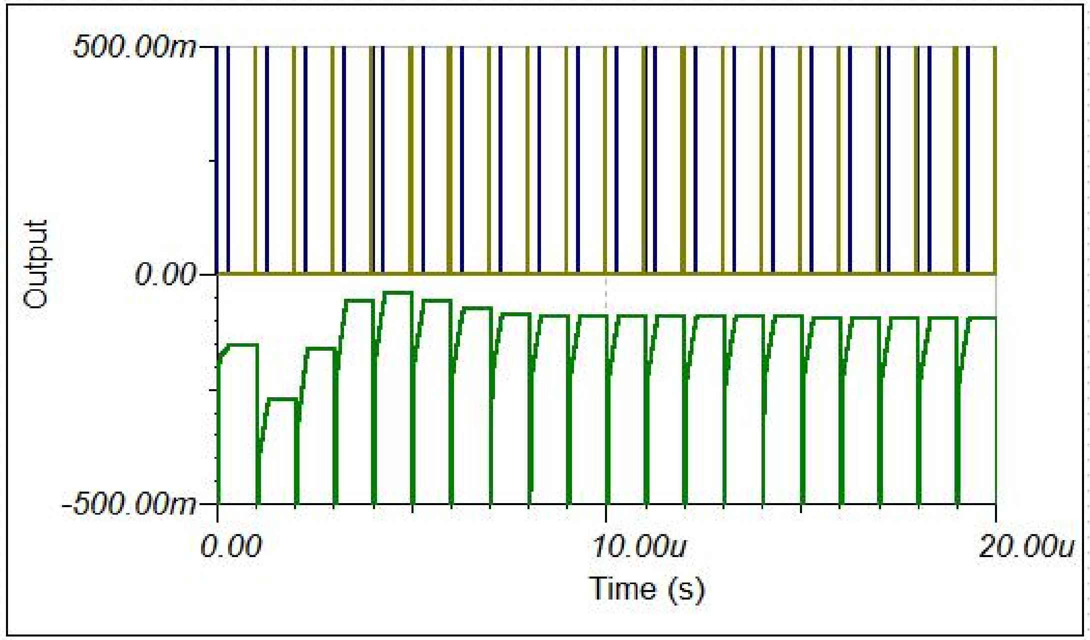
$\tau_c = \sqrt{(\tau_{RC})^2 + (\tau_{OA})^2}$	(15)	τ_c can be approximated as the RSS of the time constant of the filter and the op amp.
$\tau_{RC} = 4 \cdot \tau_{OA}$	(16)	Rule of thumb for good settling
$\tau_c = \sqrt{(4 \cdot \tau_{OA})^2 + (\tau_{OA})^2}$	(17)	Substitute (16) into (15)
$\tau_{OA} = \frac{\tau_c}{\sqrt{17}}$	(18)	Solve (17)
$\tau_{RC} = 4 \cdot \left(\frac{\tau_c}{\sqrt{17}}\right)$	(19)	Substitute (18) into (16)
$R_{filt} = \frac{\tau_{RC}}{C_{filt}}$	(20)	Nominal filter resistance.
$\boldsymbol{R_{filt\_min} = 0.25 \cdot R_{filt}}$	**(21)**	**Minimum value of Rfilt used in SPICE iteration**
$\boldsymbol{R_{filt\_max} = 2 \cdot R_{filt}}$	**(22)**	**Maximum value of Rfilt used in SPICE iteration**
$\boldsymbol{UGBW = \frac{1}{2 \cdot \pi \cdot \tau_{OA}}}$	**(23)**	**Minimum amplifier bandwidth**

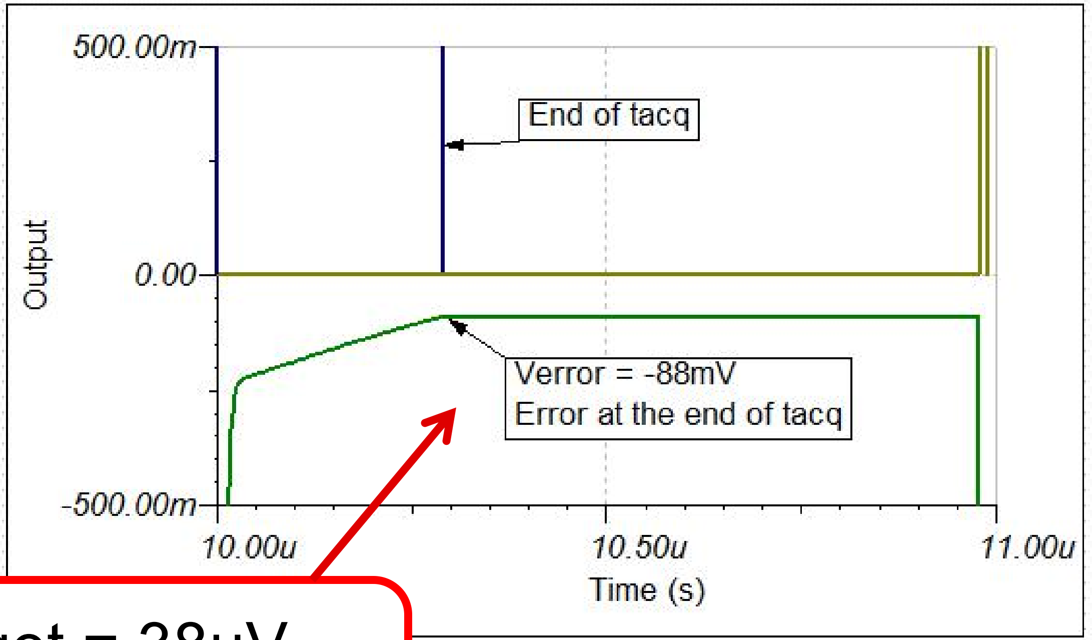
Low Bandwidth Op-amp Experiment

3: OPA333 Low Bandwidth



ADS8860_OPA333 - Low Bandwidth.TSC



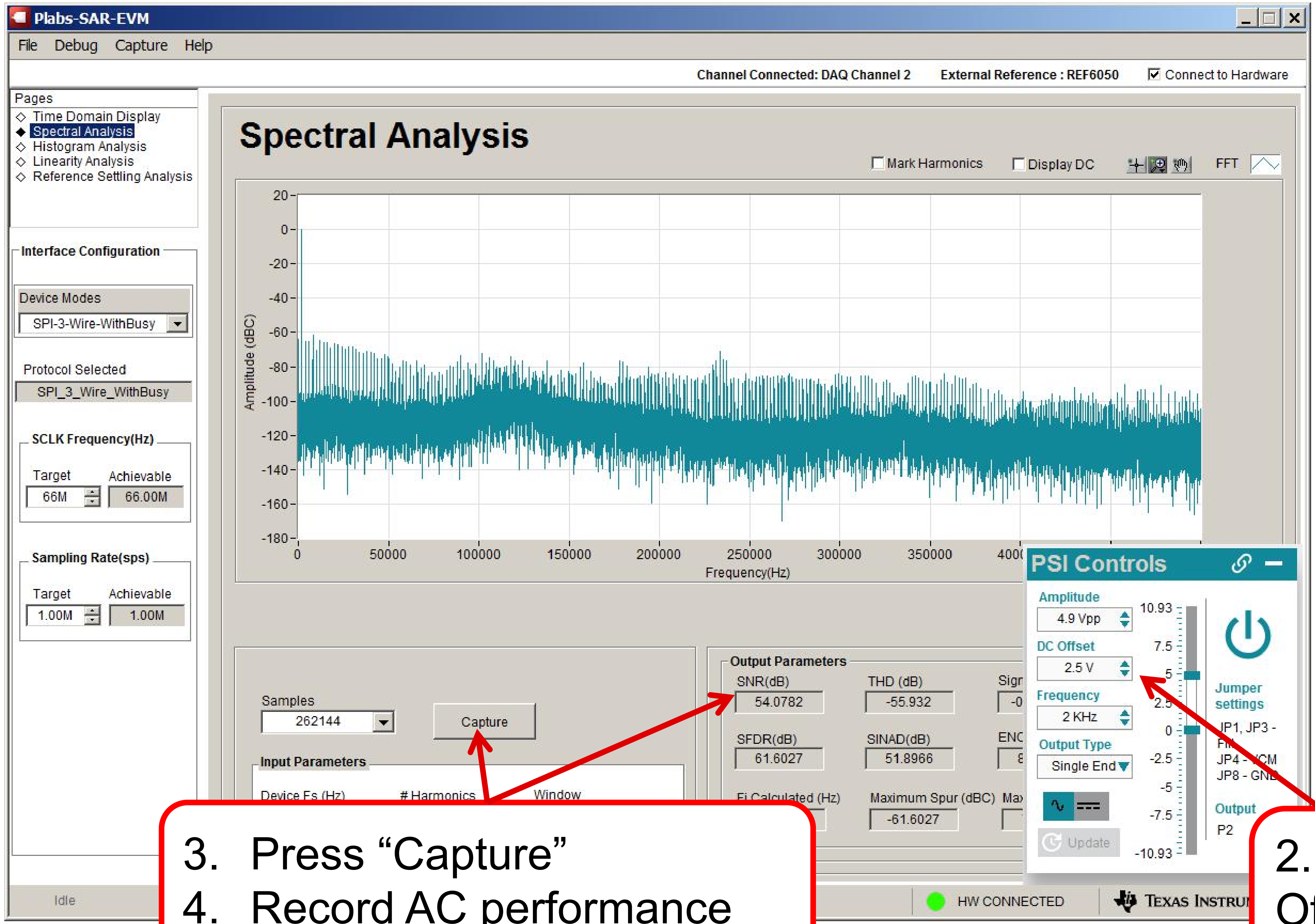


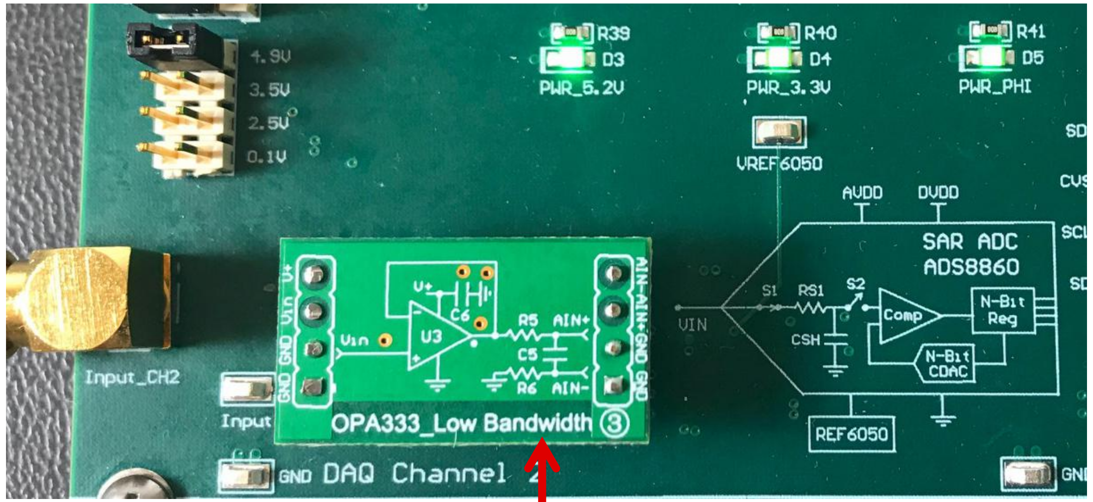
Bandwidth Required:
Gain Bandwidth= 17.8MHz
OPA333 Bandwidth:
Gain Bandwidth= 350kHz

Error Target = 38µV
Simulate Error = -88mV

3: OPA333 Low Bandwidth

	SNR (dB)	THD (dB)
ADS8860	93	-108
Low Bandwidth	54.1	-55.9





1. Install OPA333_Low Bandwidth coupon card in socket.

2. Amplitude = 4.9V
Offset = 2.5V
Frequency = 2kHz

3. Press “Capture”
4. Record AC performance

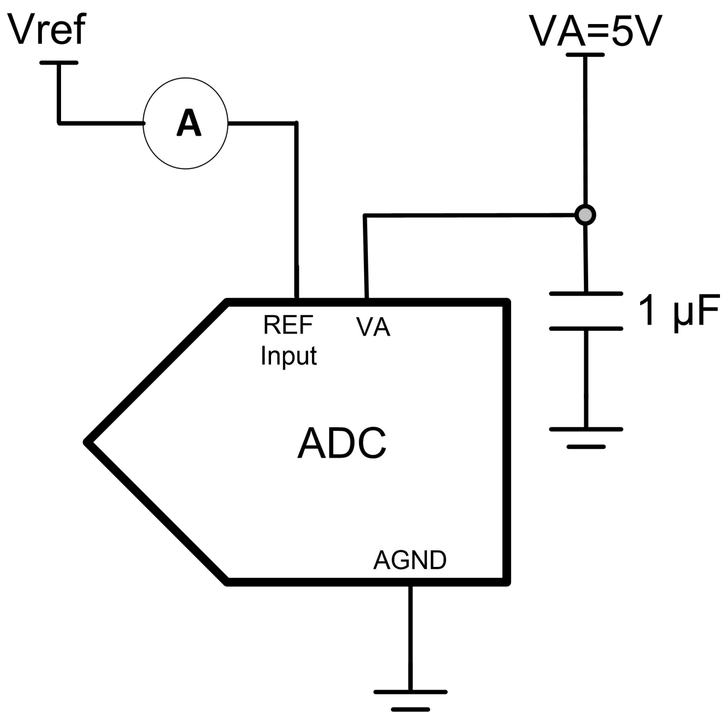
Measured vs Expected Results

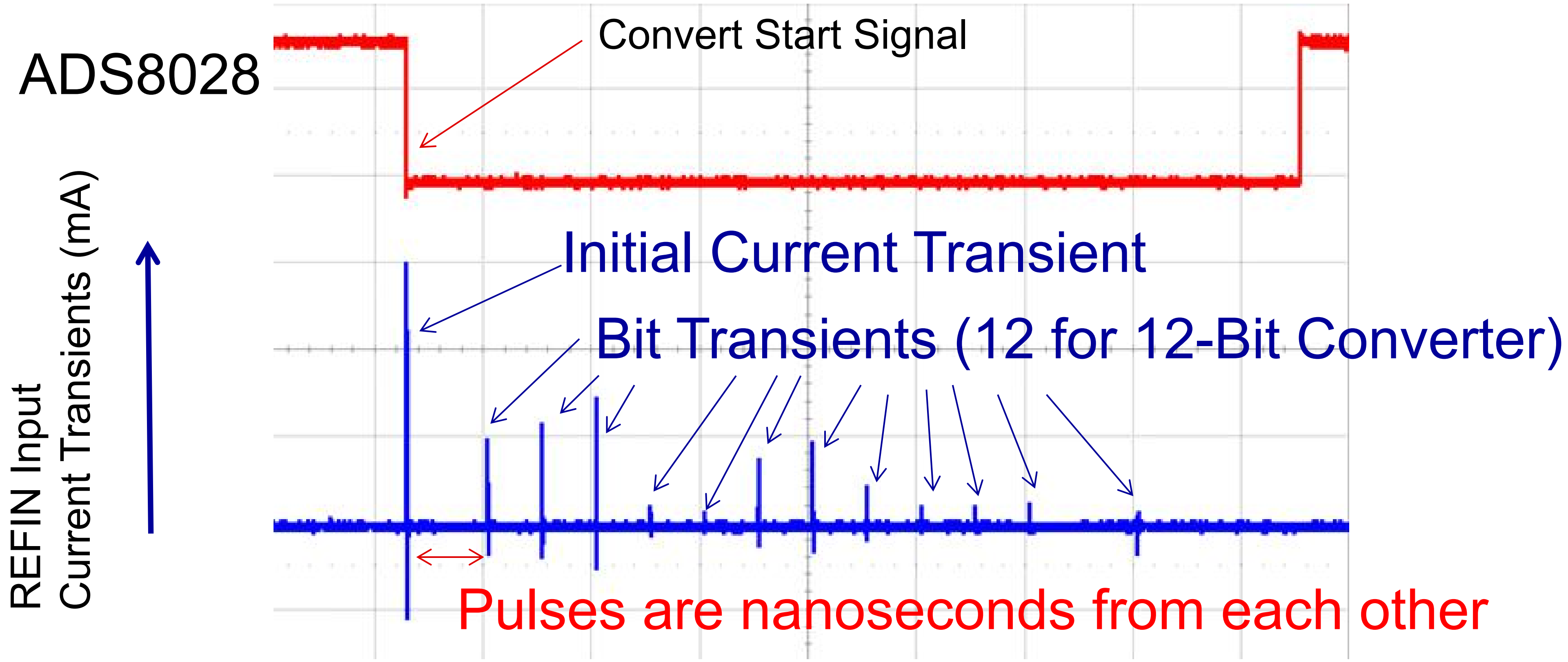
Device					Simulated Settling Error ½LSB=38uV	Example Measurements	
	Device	Samp.Rate	V_{offset} (V)	V_{in} (V)	V_{error} (V)	SNR (dB)	THD (dB)
	ADS8860 Data Sheet					93	-108
1	OPA320 Good filter1	1M	2.5	4.9	28uV	93.3	-108.8
2	OPA320 Bad filter	1M	2.5	4.9	-41mV	82.5	-73.4
3	OPA333 Low Bandwidth	1M	2.5	4.9	-91mV	54.1	-55.9
4	OPA316 Crossover	1M	1.8	3.6	36.7mV	86.1	-85.0

How Voltage Reference Affecting ADC System

Speaker: Andrew Wang

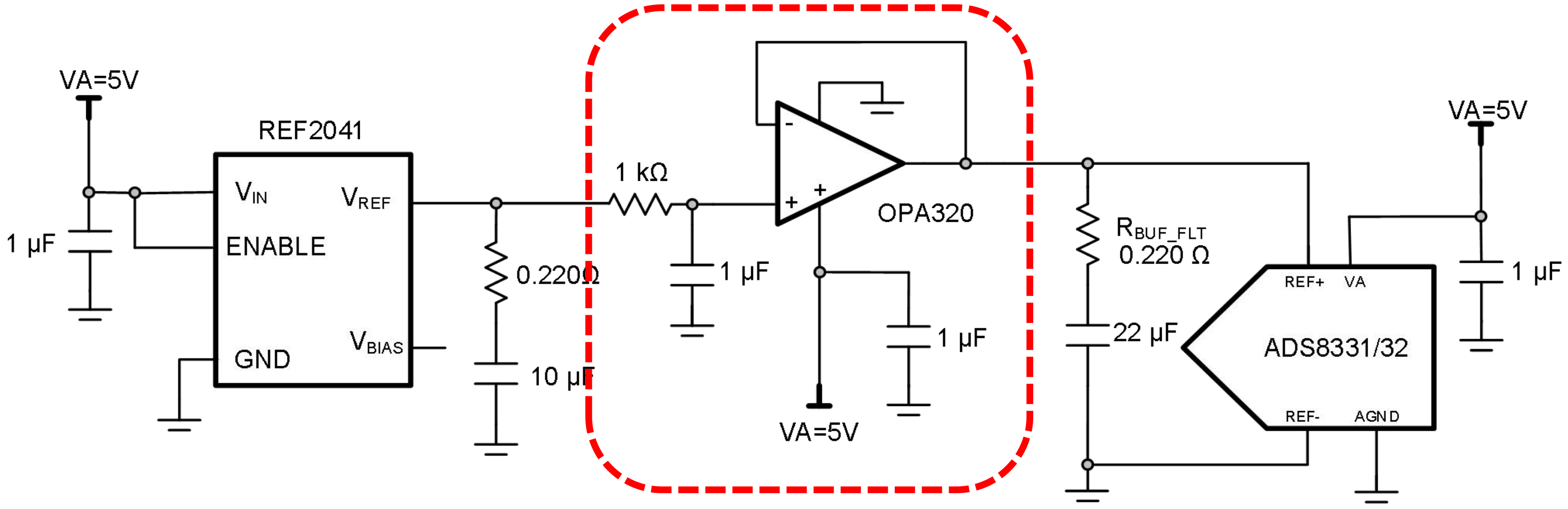
ADC Reference input is not a high impedance



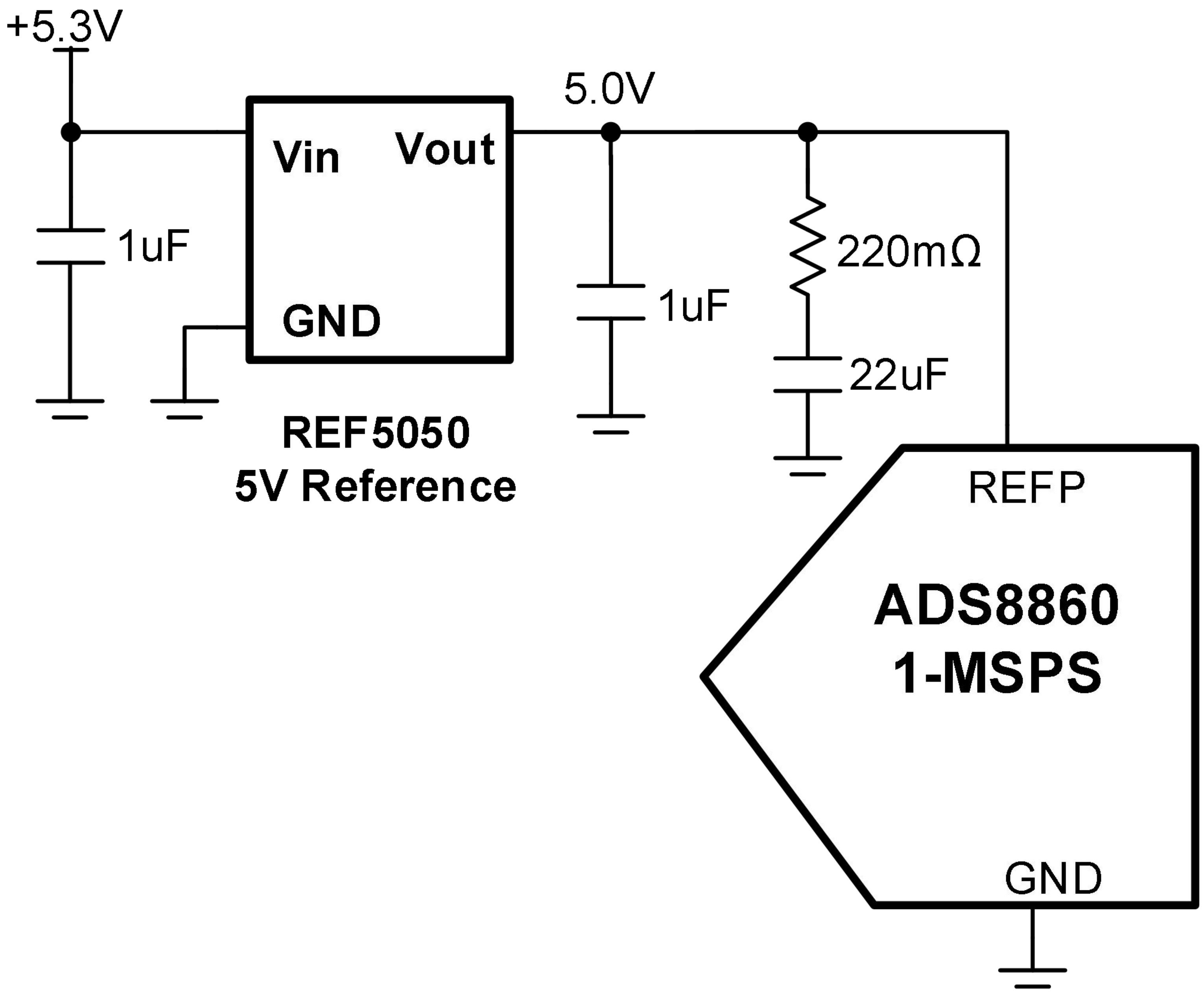


What is a reference buffer?

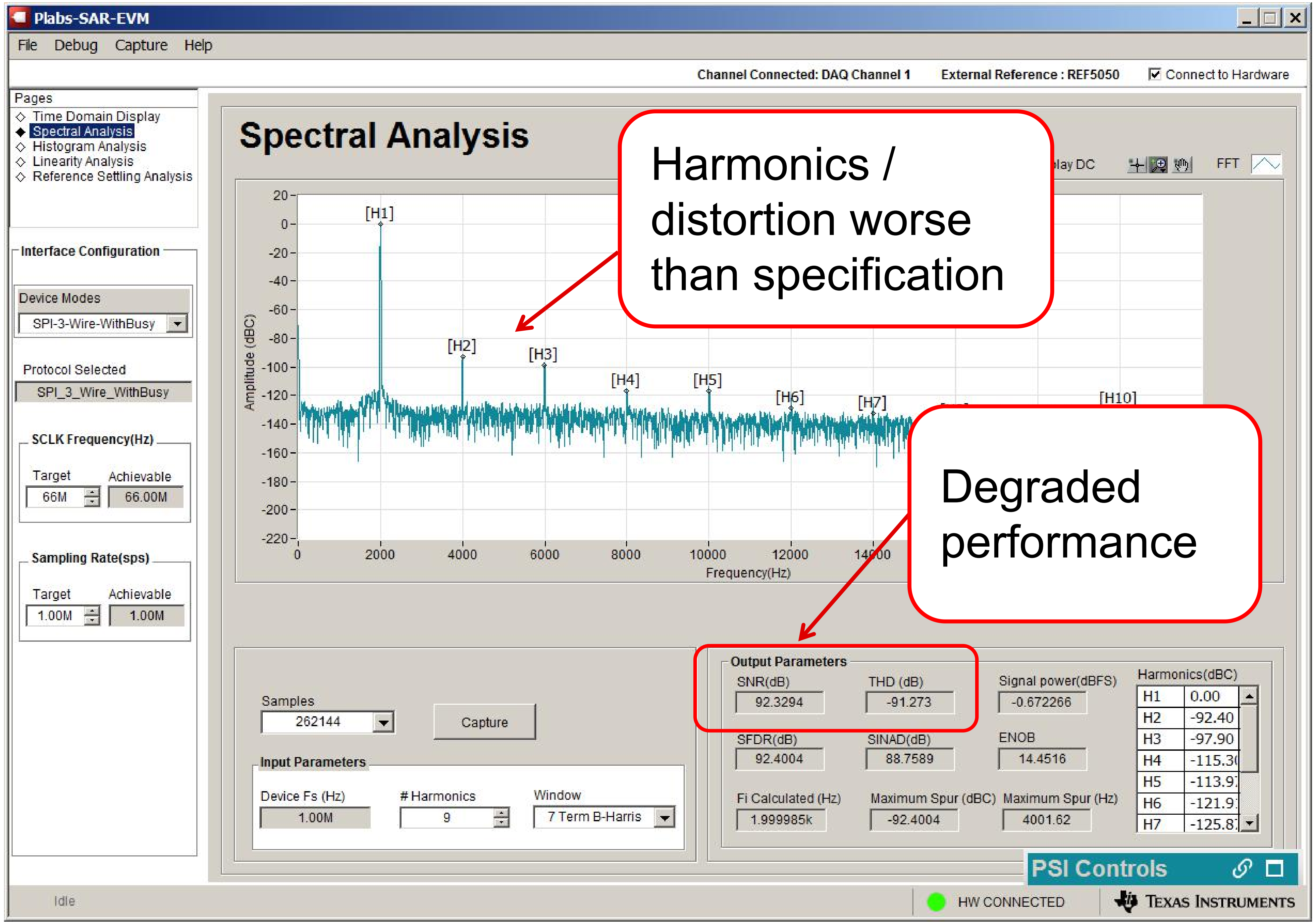
- Wide bandwidth
- Low output impedance across frequency
- Capable of sourcing and relatively large currents (e.g. ±10mA)
- Good DC specifications (i.e. offset, and Temperature Drift)
- May be integrated in the reference, or an external amplifier



Performance limitations from unbuffered reference

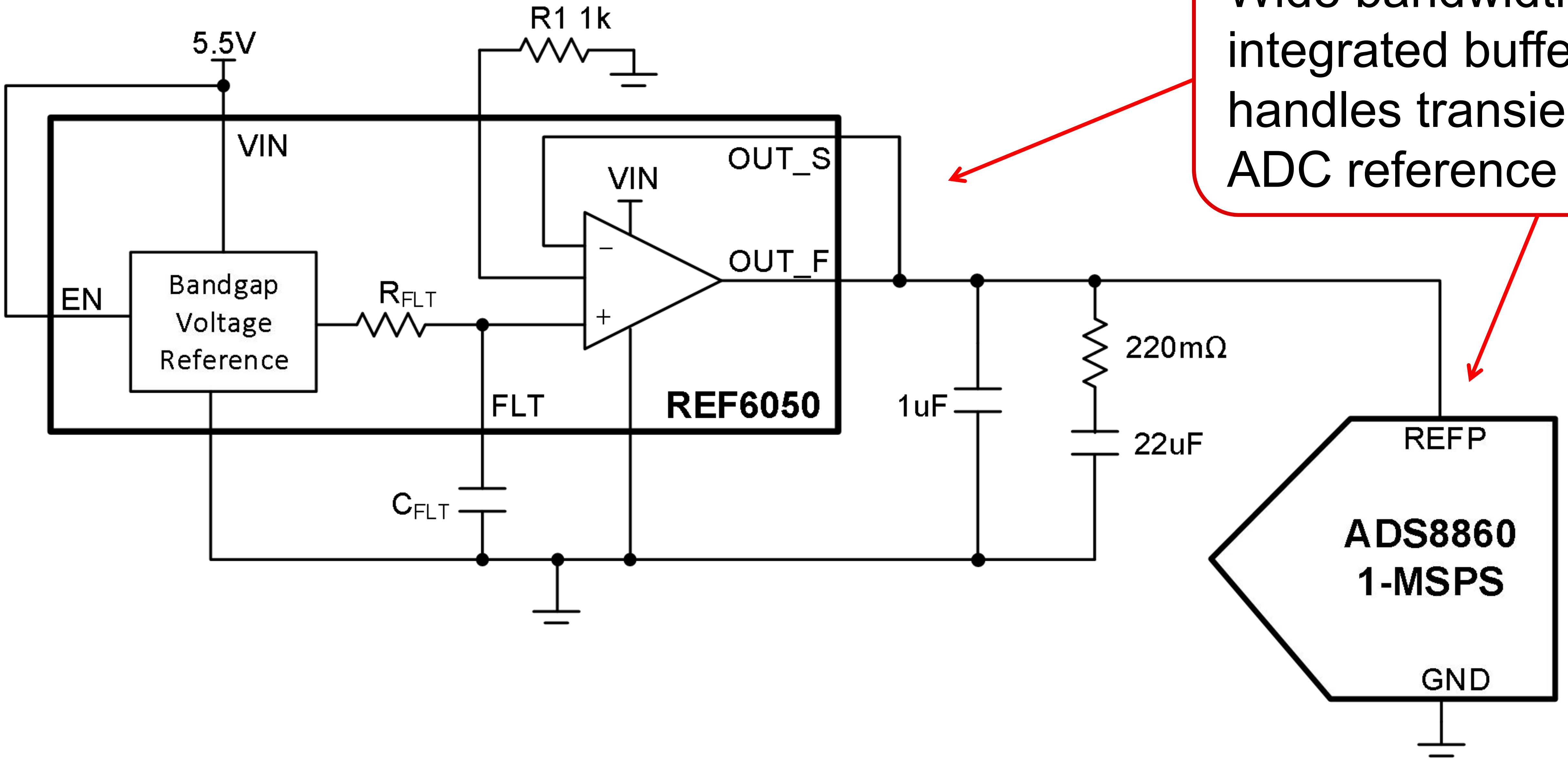


Unbuffered Reference: ADS8860 + REF5050



	SNR (dB)	THD (dB)
Specification	93	-108
REF5050	92.3	-91.3

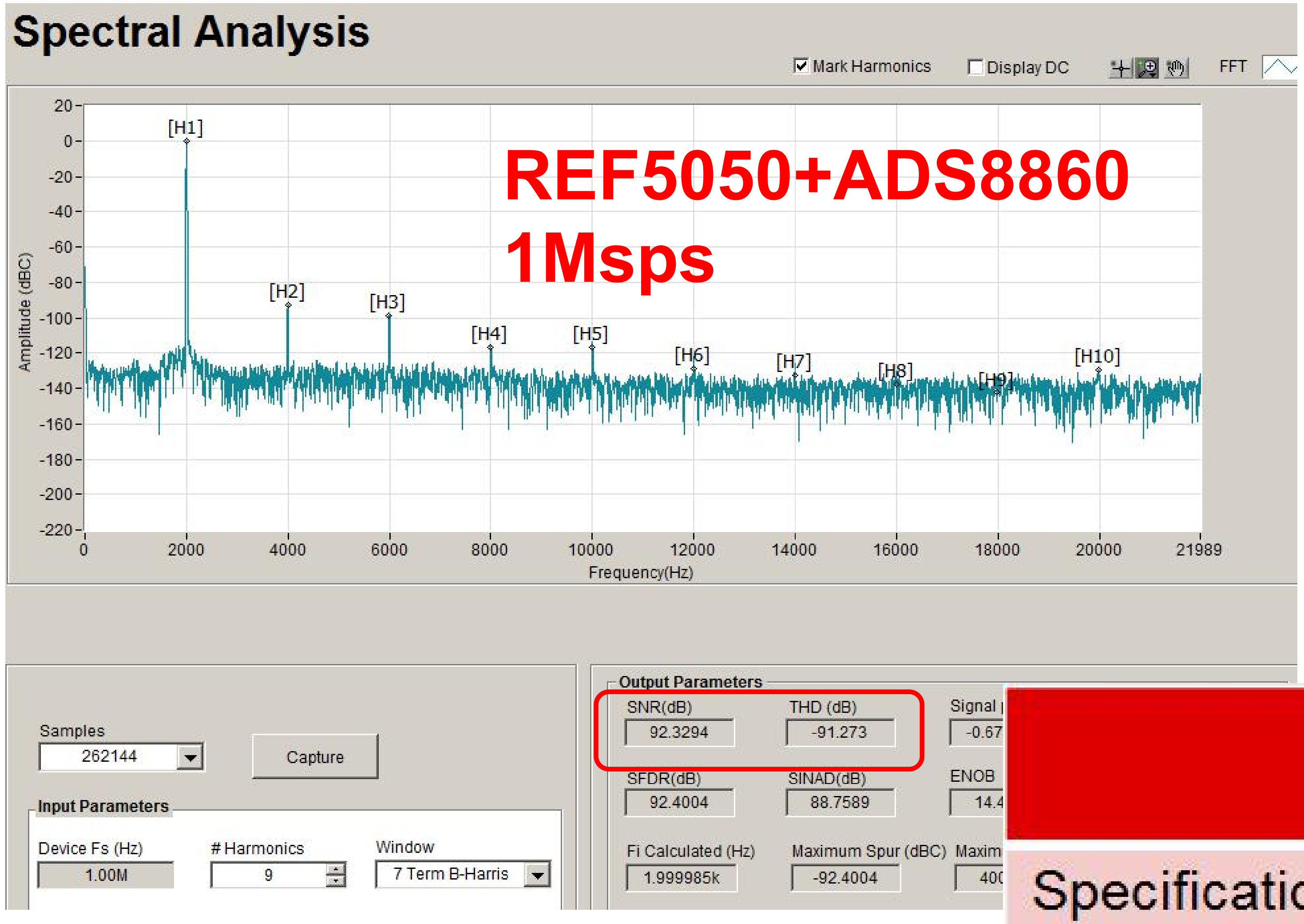
Performance improvement using buffered reference

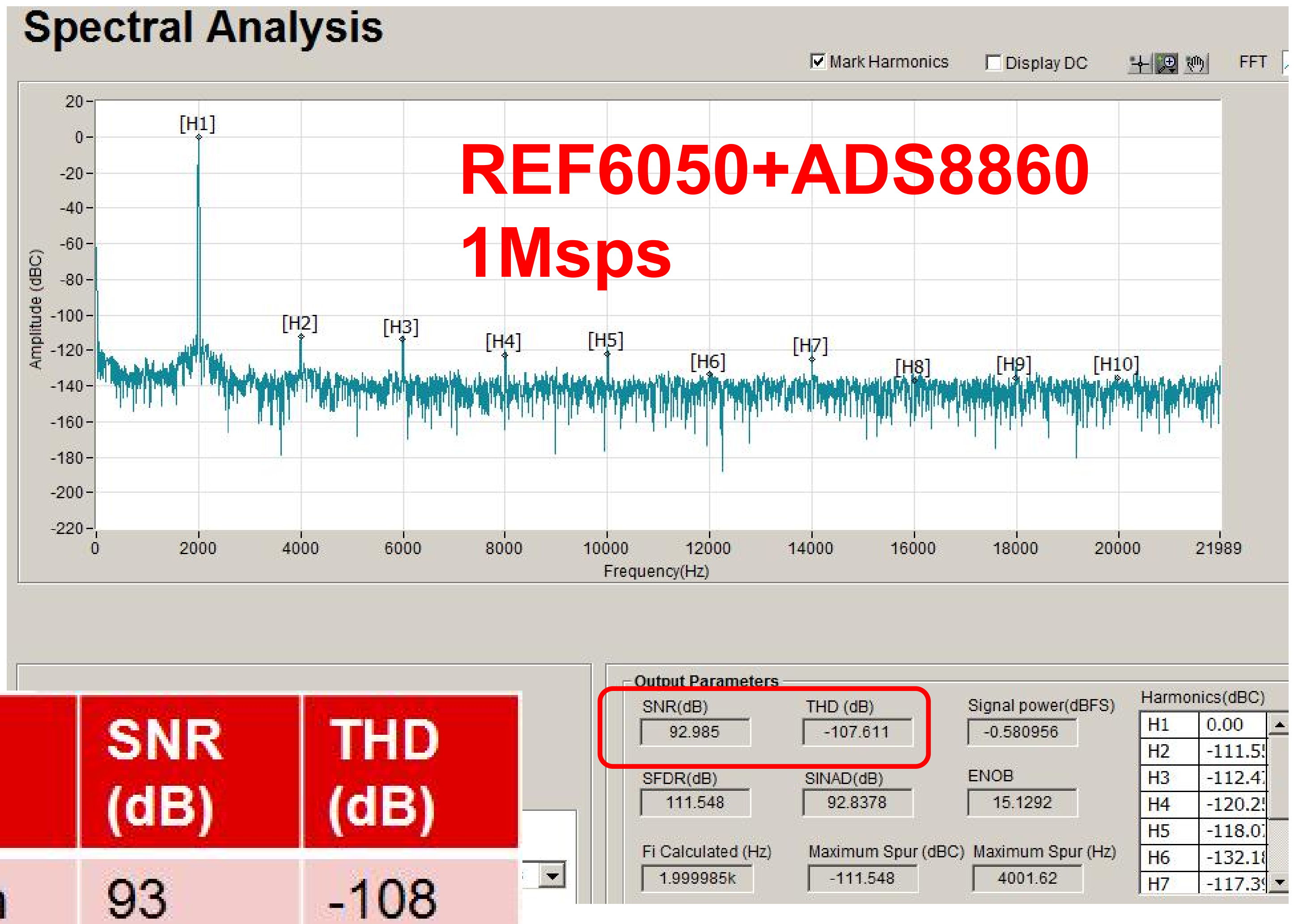


Wide bandwidth integrated buffer handles transients from ADC reference input

Demo – SNR / THD difference

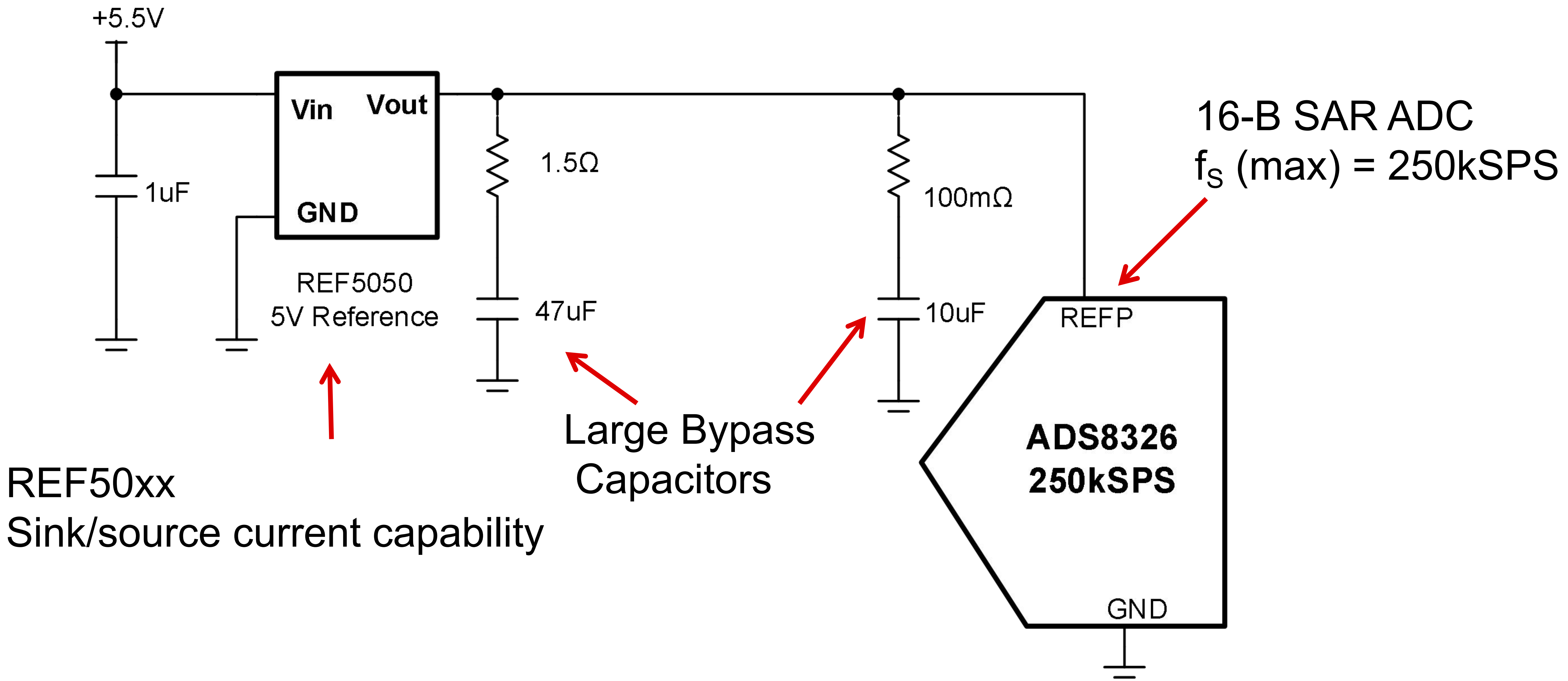
Buffered vs. Unbuffered.





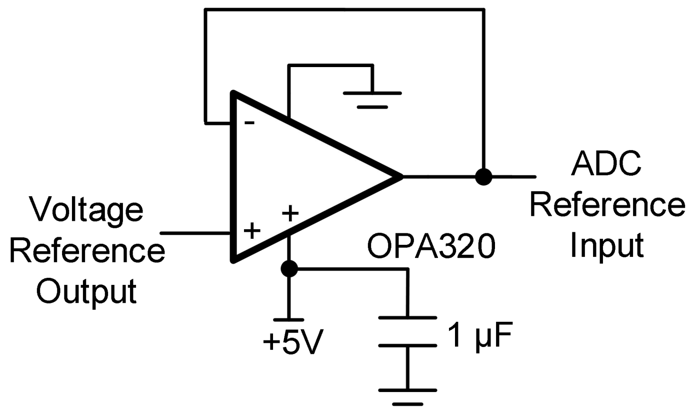
	SNR (dB)	THD (dB)
Specification	93	-108
REF5050	92.3	-91.3
REF6050	92.9	-107.6

Buffered reference isn't always required

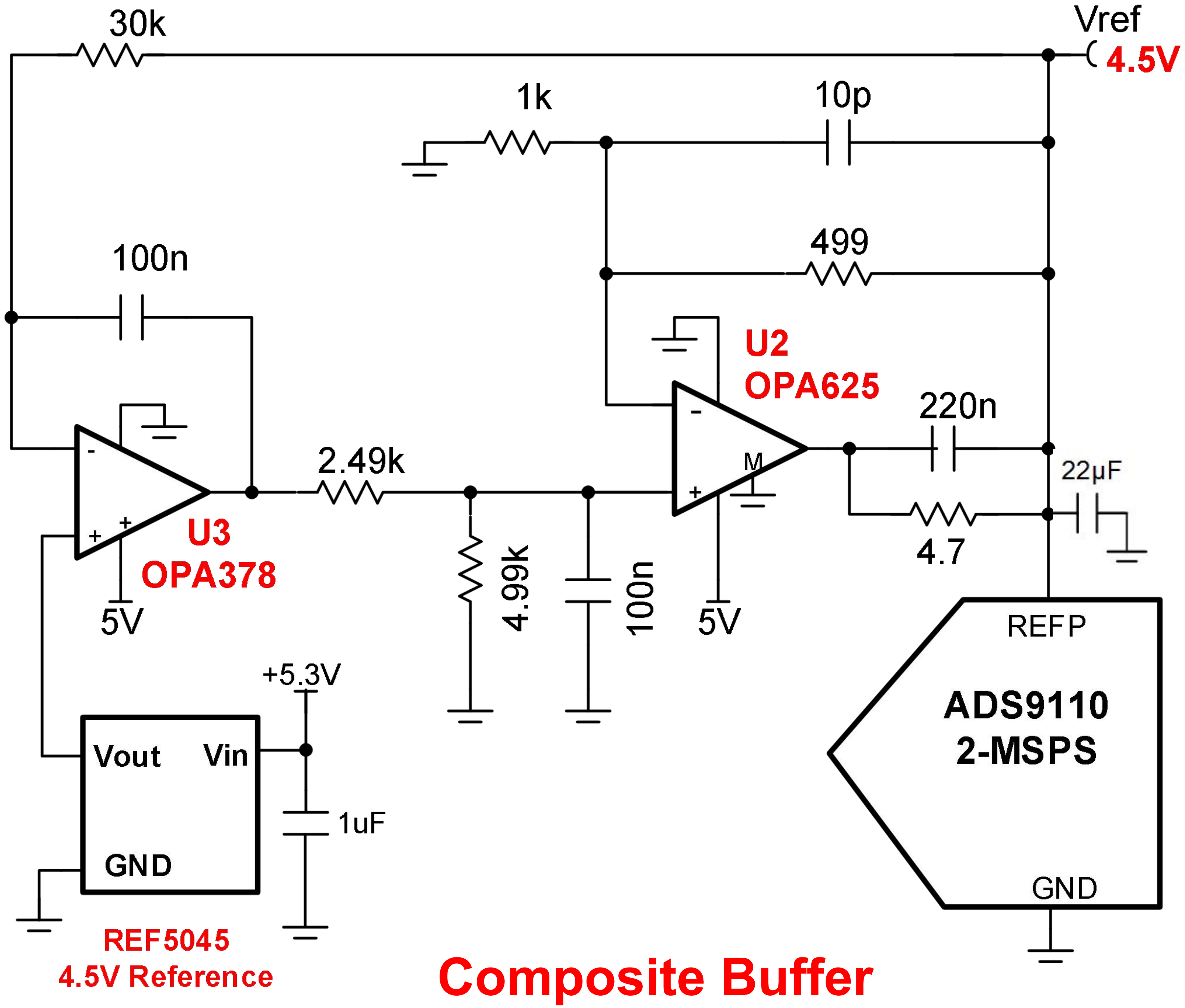


Composite Amplifier Topology

- OPA378 chopper op-amp as an input stage for excellent low drift and DC stability of buffer.
- High-Bandwidth output buffer (OPA625) provides and wide bandwidth and low-output impedance to drive the SAR REFP input

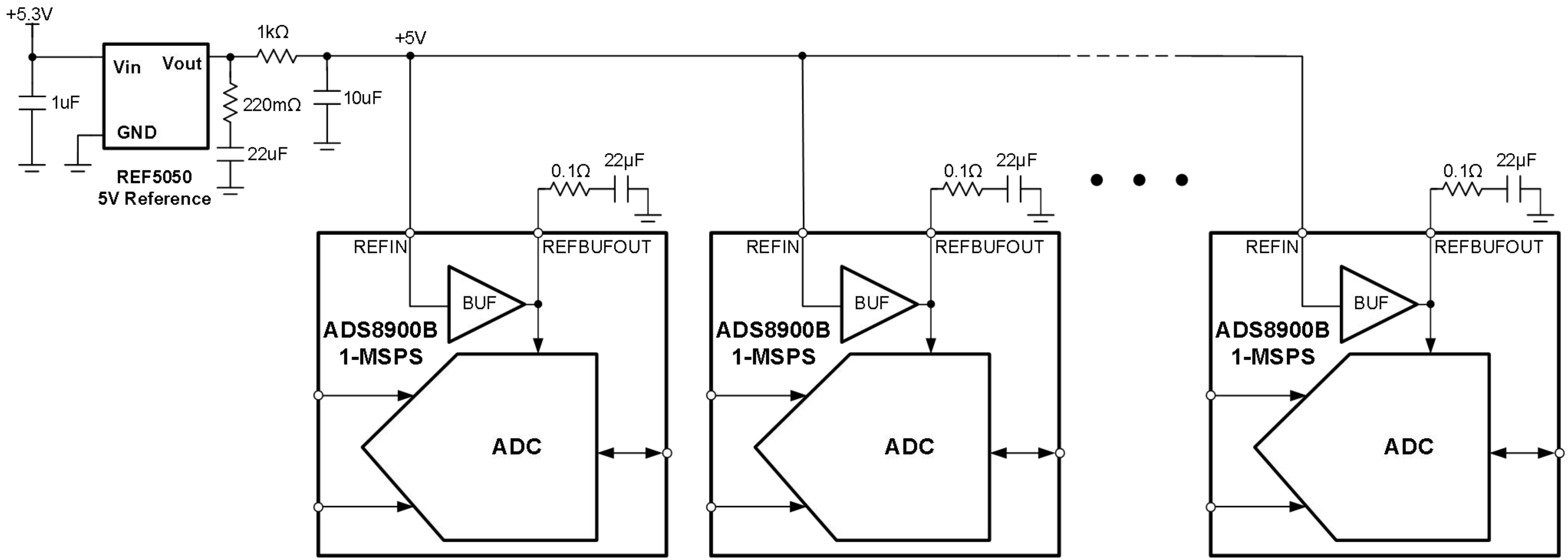


Simple Buffer



Composite Buffer

Device with internal reference buffer: ADS89xxB

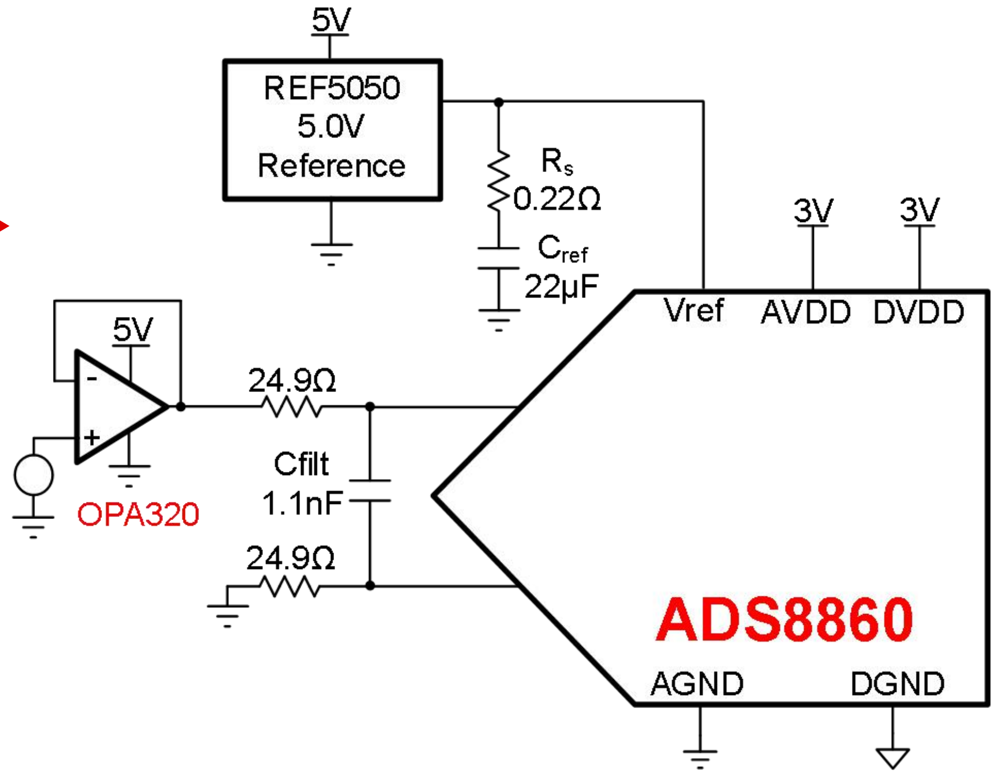


Voltage Reference Experiment

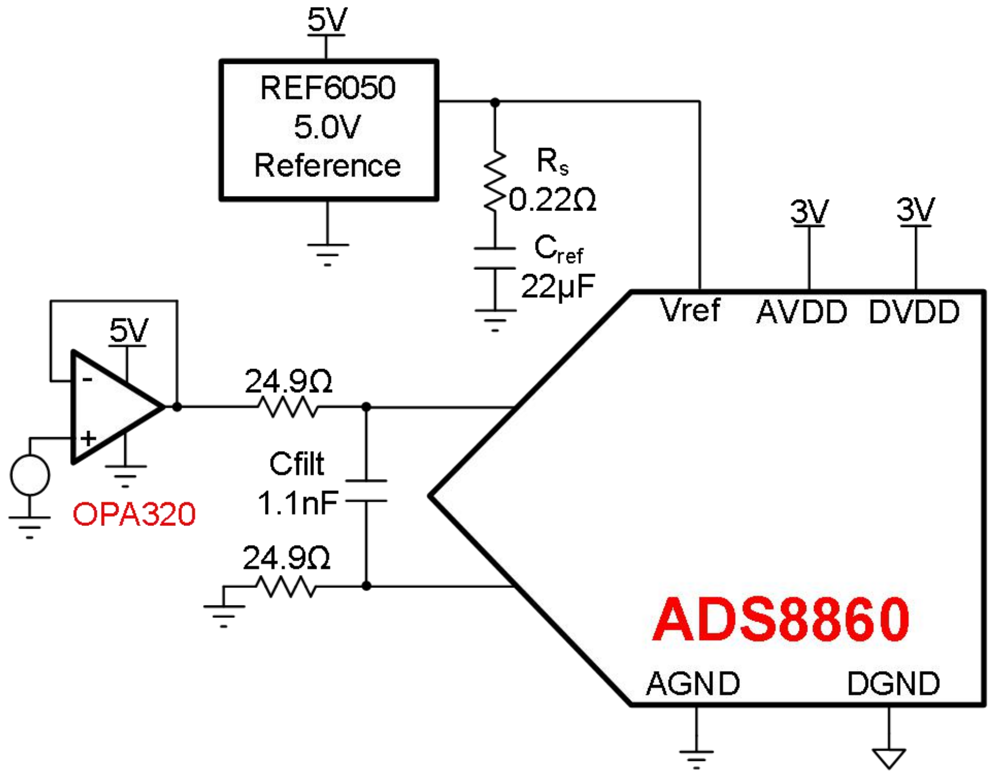
Circuits under test

Circuits are identical except for the reference.

Channel 1: REF5050



Channel 2: REF6050



ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD (1kHz)		-108		dB

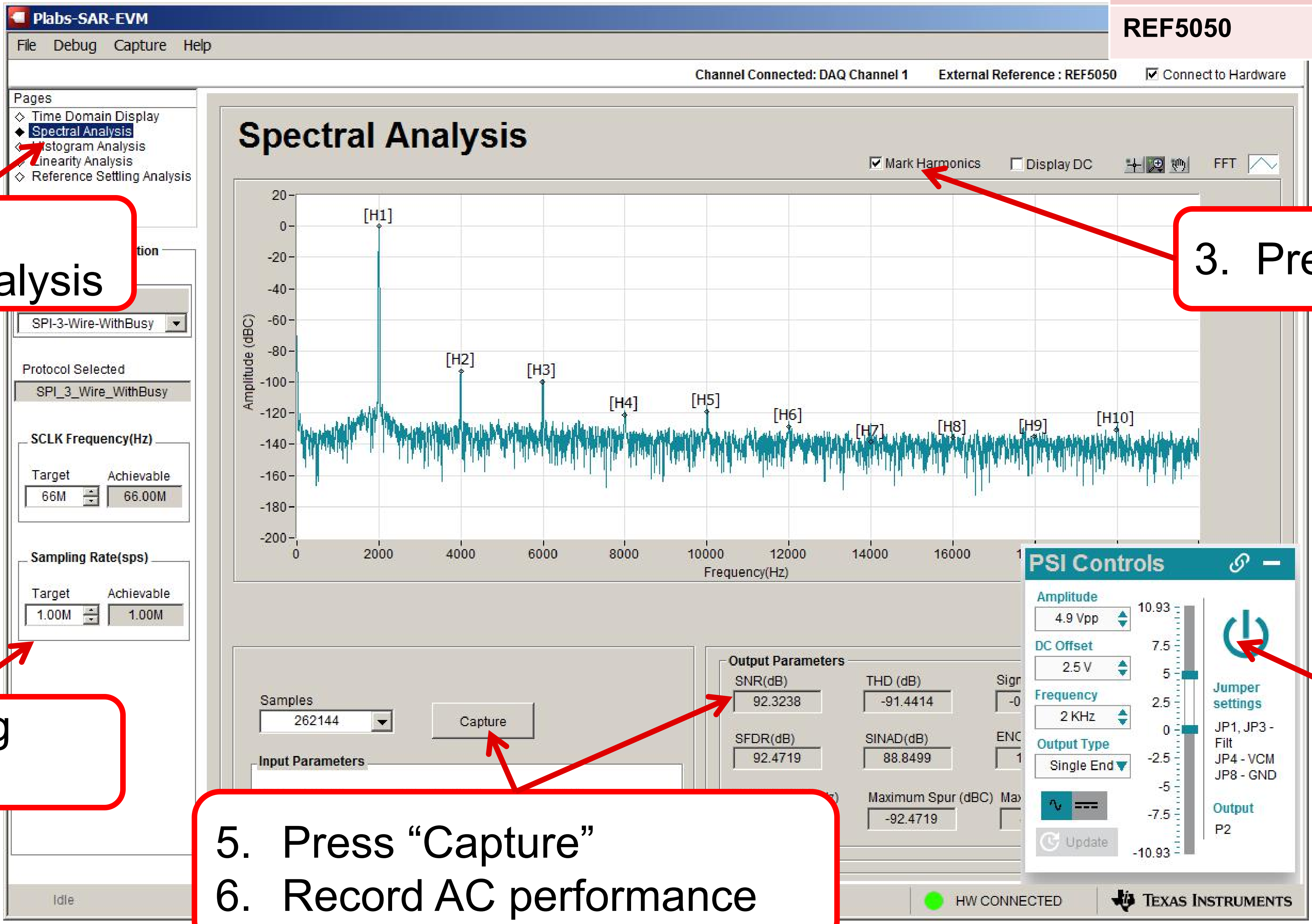
Should meet ADS8860 data sheet specifications

Expected results

Reference		Sampling Rate	Example Measurements		
			SNR (dB)	THD (dB)	Reference Droop Vin = 4.9V DC (codes)
	Data Sheet Typical Specification	1M	93	-108	
1	REF5050	1M	92.2	-91.4	10.9
2	REF5050	500k	92.1	-97.1	5.35
3	REF5050	100k	92.0	-108.2	1.4
4	REF6050	1M	92.6	-108.1	1.15
5	REF6050	500k	92.7	-109.3	0.8
6	REF6050	100k	92.3	-108.1	0.8

REF5050: 1Msps, THD, SNR

	fs	SNR (dB)	THD (dB)
Spec.	1M	93	-108
REF5050	**1M**	**92.2**	**-91.4**



1. Select spectral analysis

2. Sampling Rate 1Msps

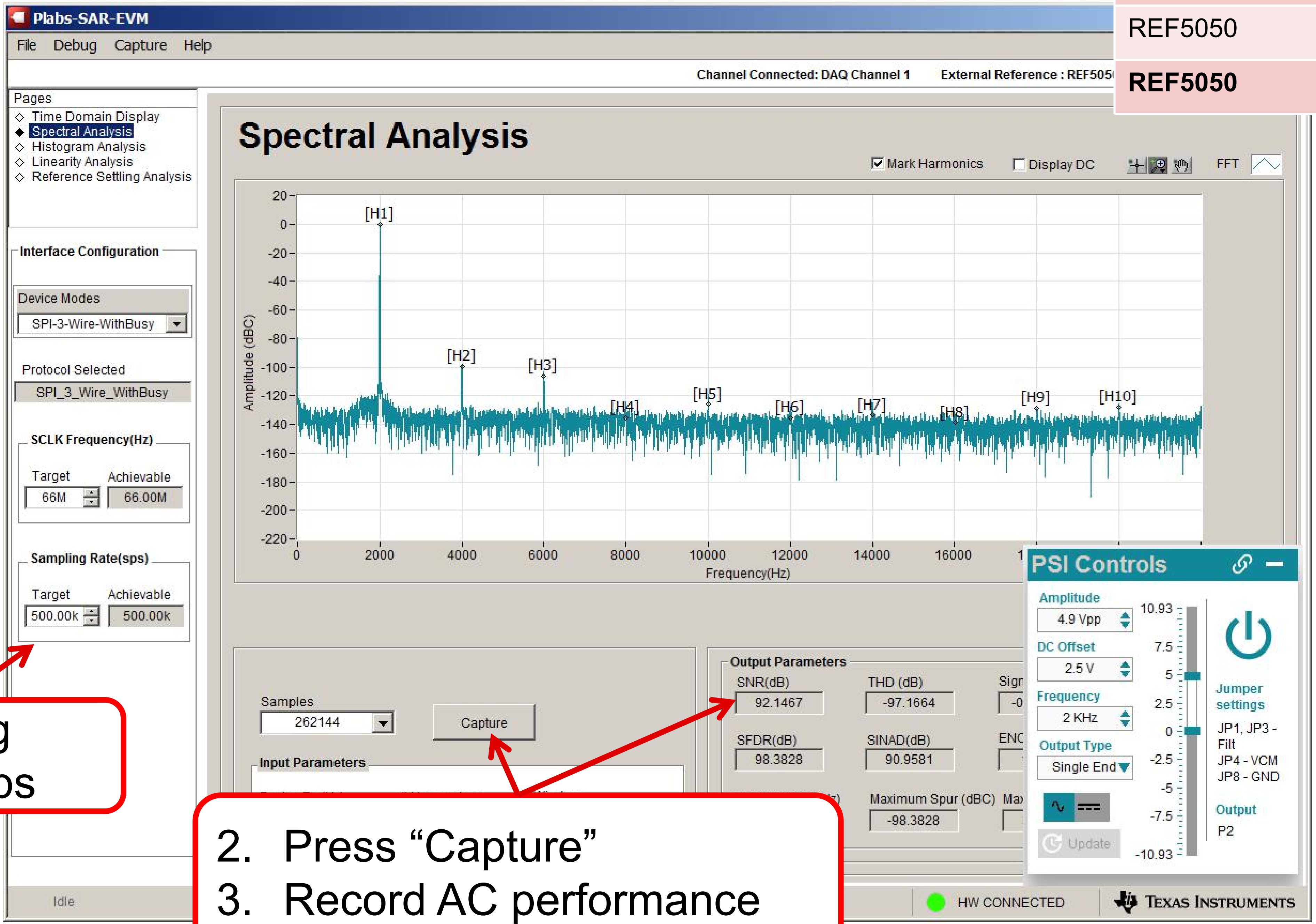
3. Press Mark Harmonics

4. Amplitude = 4.9V
Offset = 2.5V
Frequency = 2kHz
Press power on.

5. Press “Capture”
6. Record AC performance

REF5050: 500ksps, THD, SNR

	fs	SNR (dB)	THD (dB)
Spec.	1M	93	-108
REF5050	1M	92.2	-91.4
REF5050	**500k**	**92.1**	**-97.1**

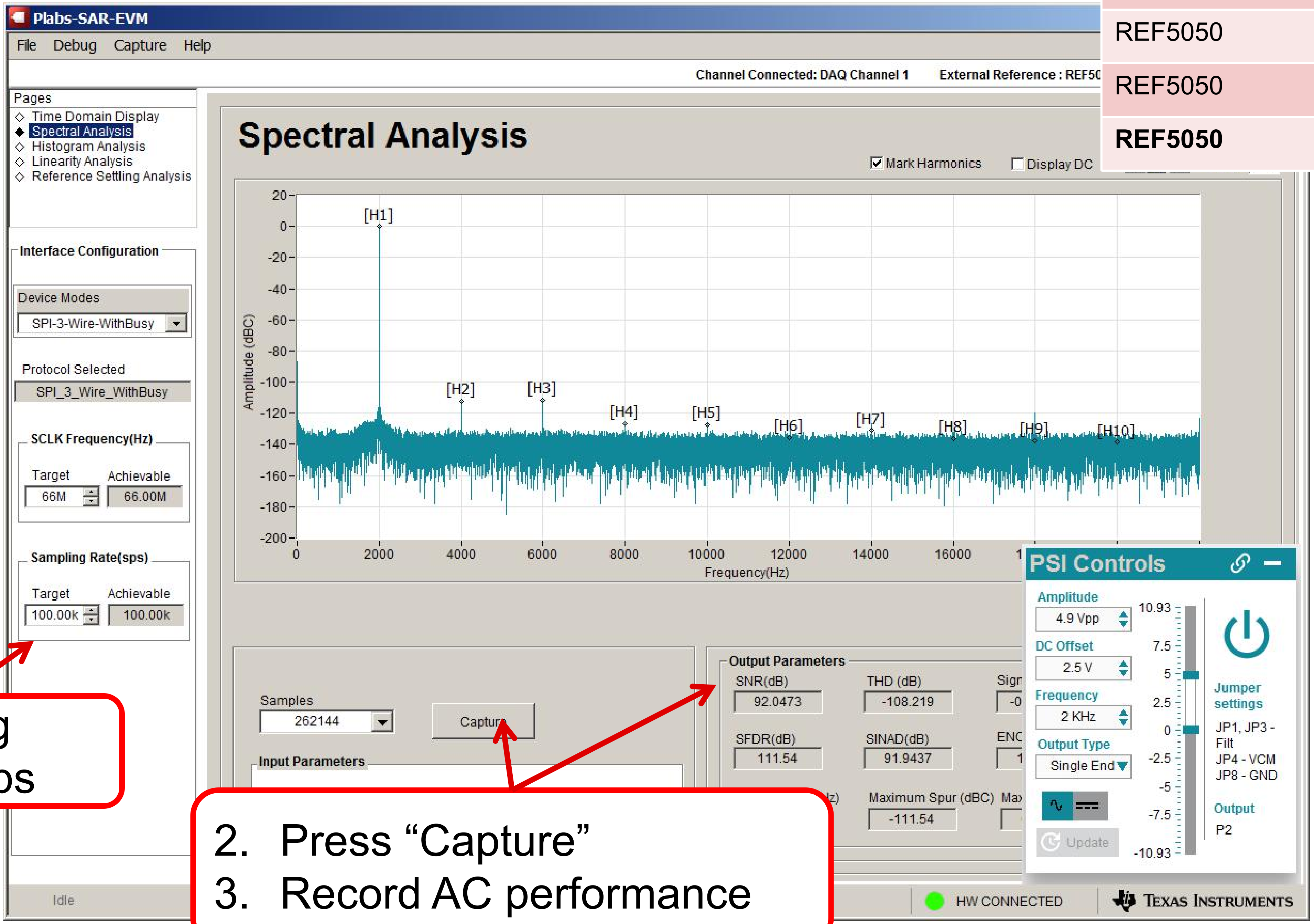


1. Sampling Rate 500ksps

2. Press “Capture”
3. Record AC performance

REF5050: 100ksps, THD, SNR

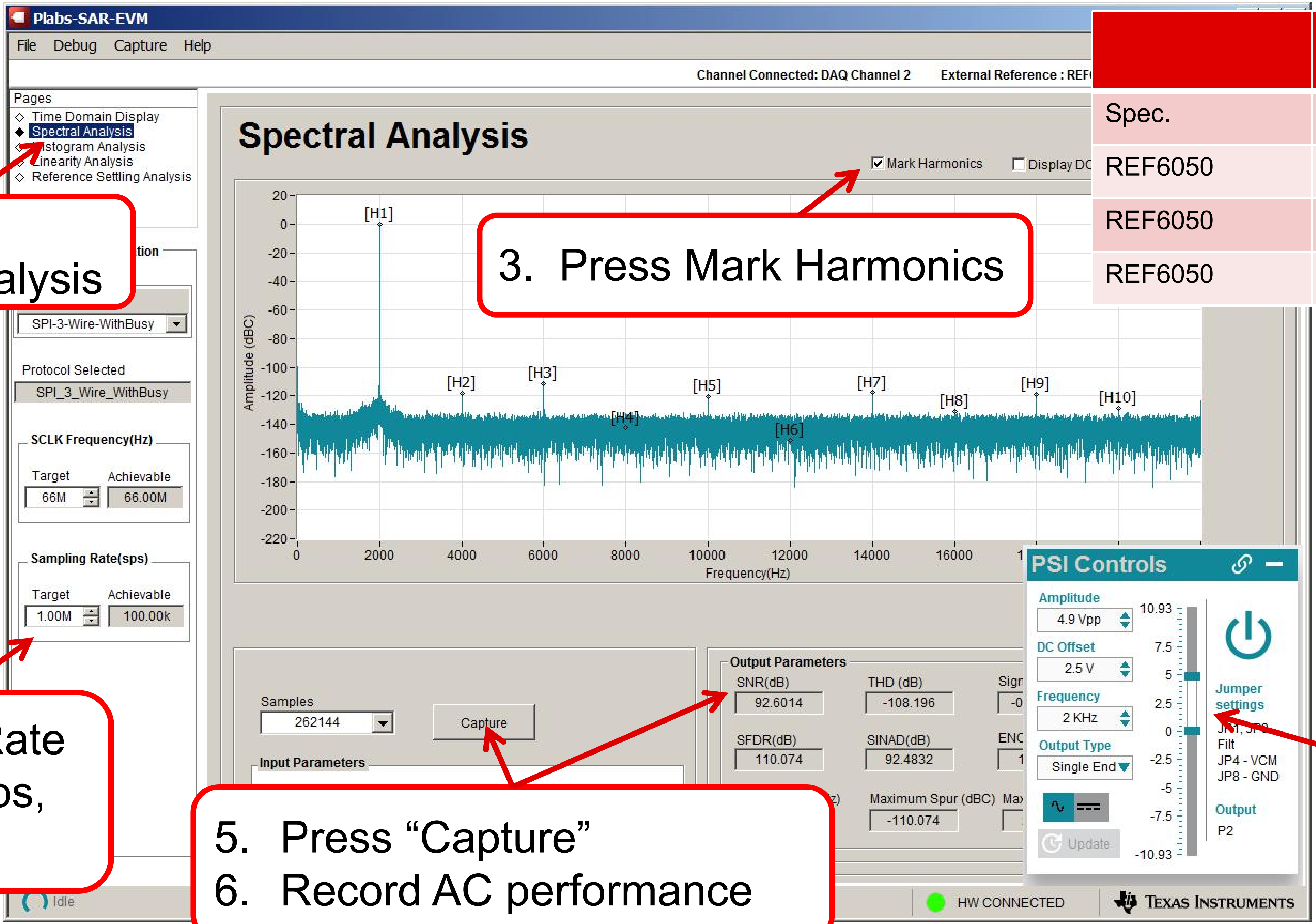
	fs	SNR (dB)	THD (dB)
Spec.	1M	93	-108
REF5050	1M	92.2	-91.4
REF5050	500k	92.1	-97.1
REF5050	**100k**	**92.0**	**-108.2**



1. Sampling Rate 100ksps

2. Press "Capture"
3. Record AC performance

REF6050: 1Msps, 500ksps, 100ksps: SNR, THD



	fs	SNR (dB)	THD (dB)
Spec.	1M	93	-108
REF6050	1M	92.6	-108.1
REF6050	500k	92.7	-109.3
REF6050	100k	92.3	-108.1

1. Select spectral analysis

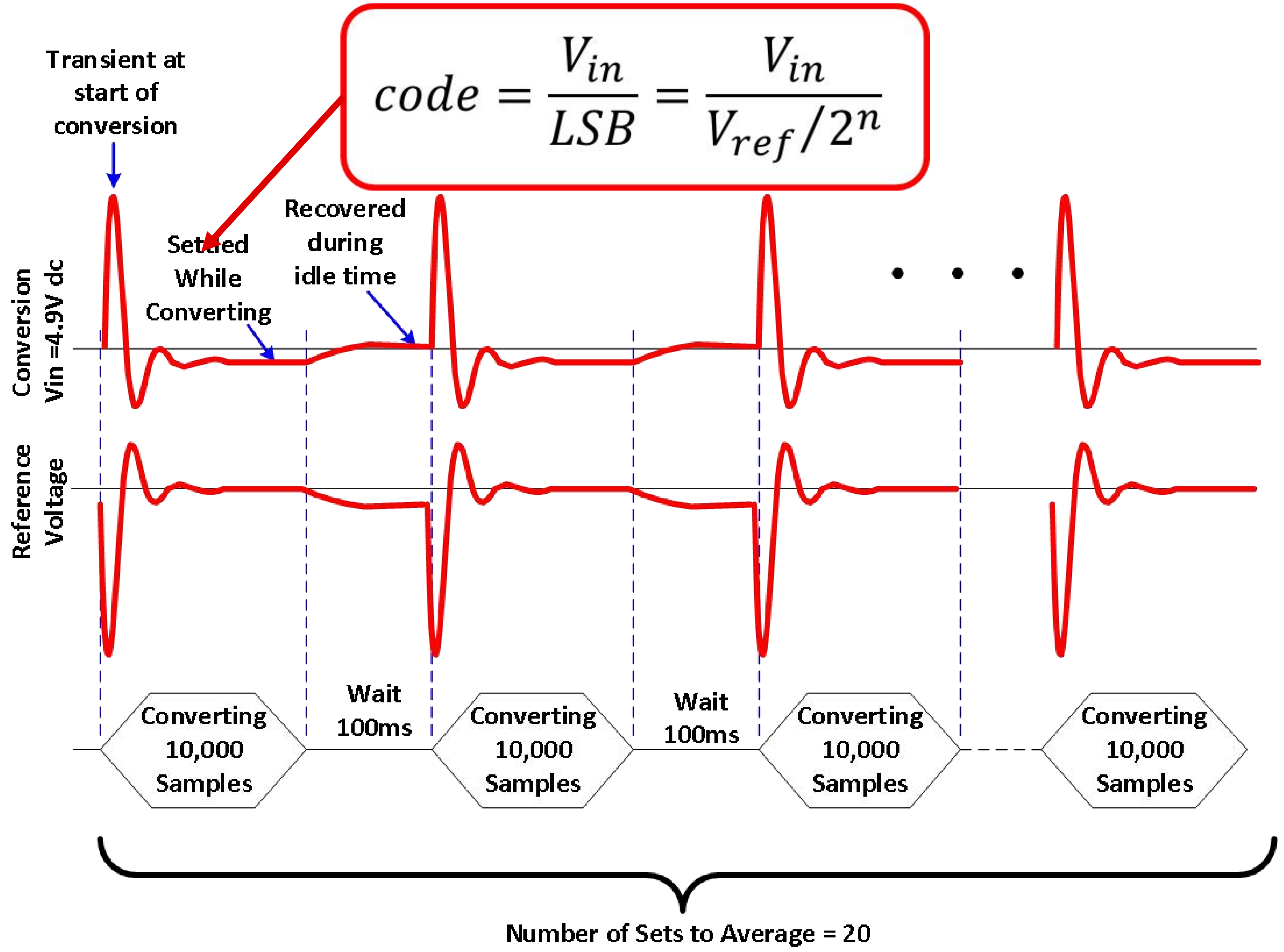
2. Sampling Rate 1Msps, 500ksps, 100ksps

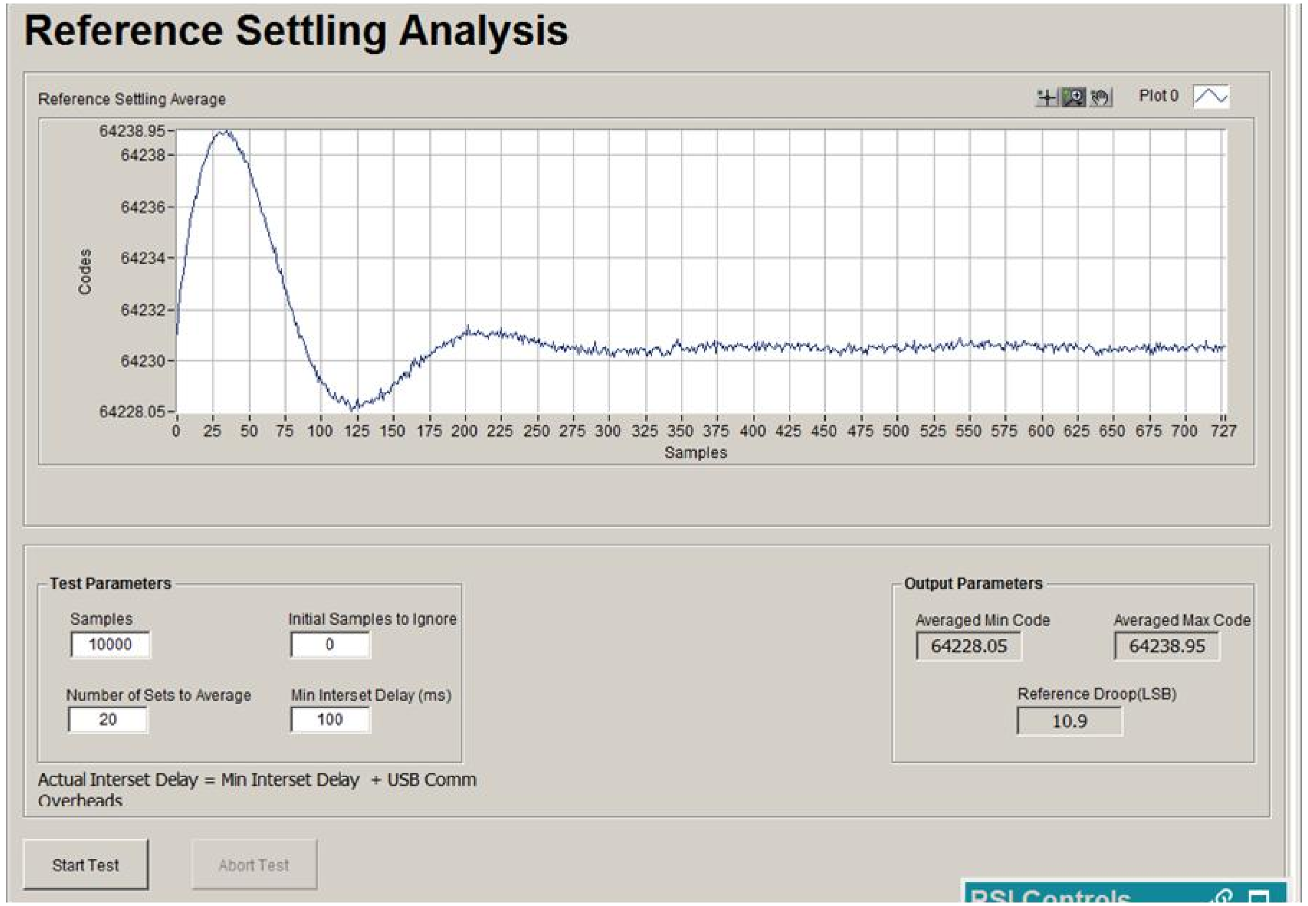
3. Press Mark Harmonics

4. Amplitude = 4.9V
Offset = 2.5V
Frequency = 2kHz

5. Press "Capture"
6. Record AC performance

Reference Settling Test

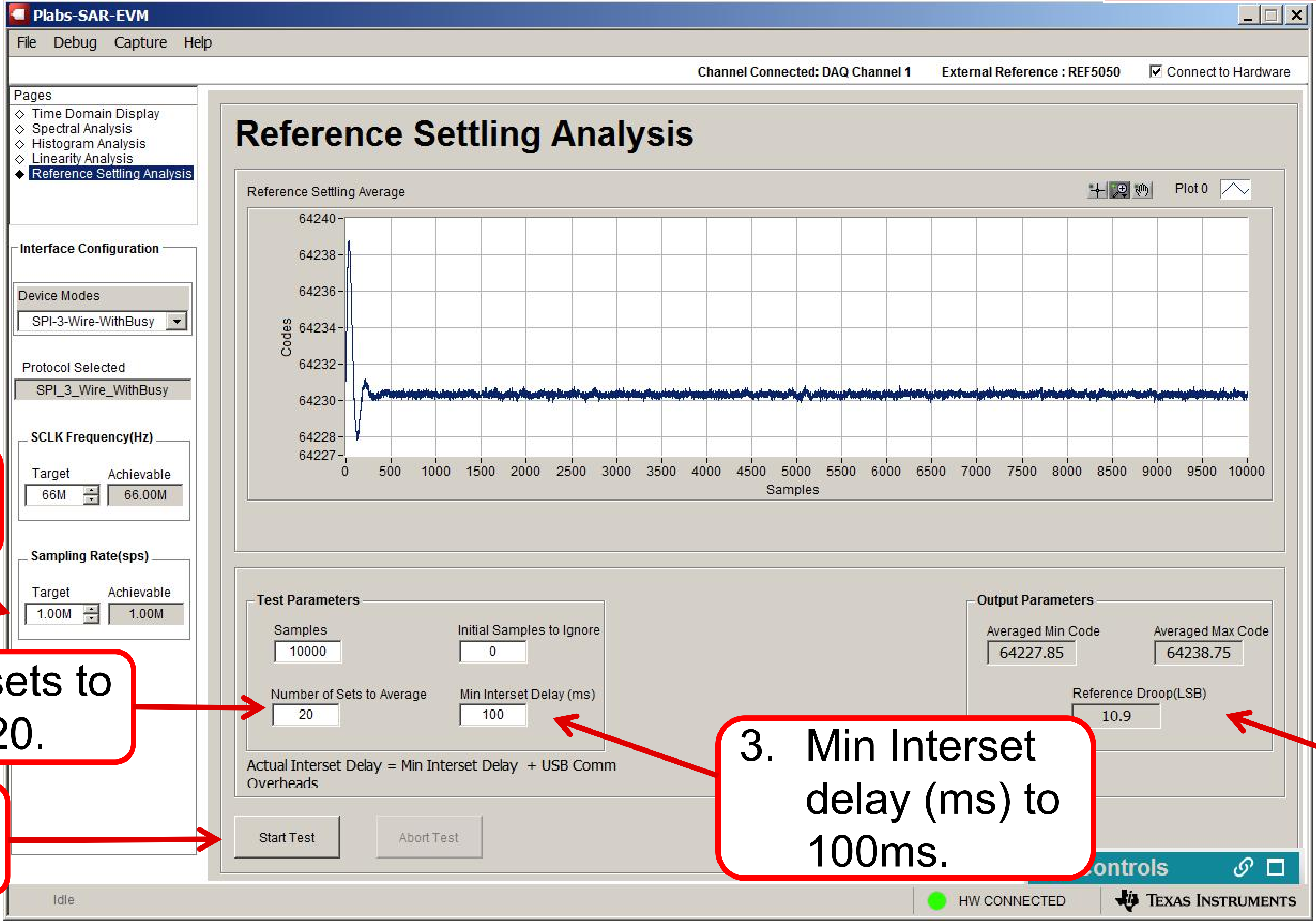




Demo – Settling Time difference

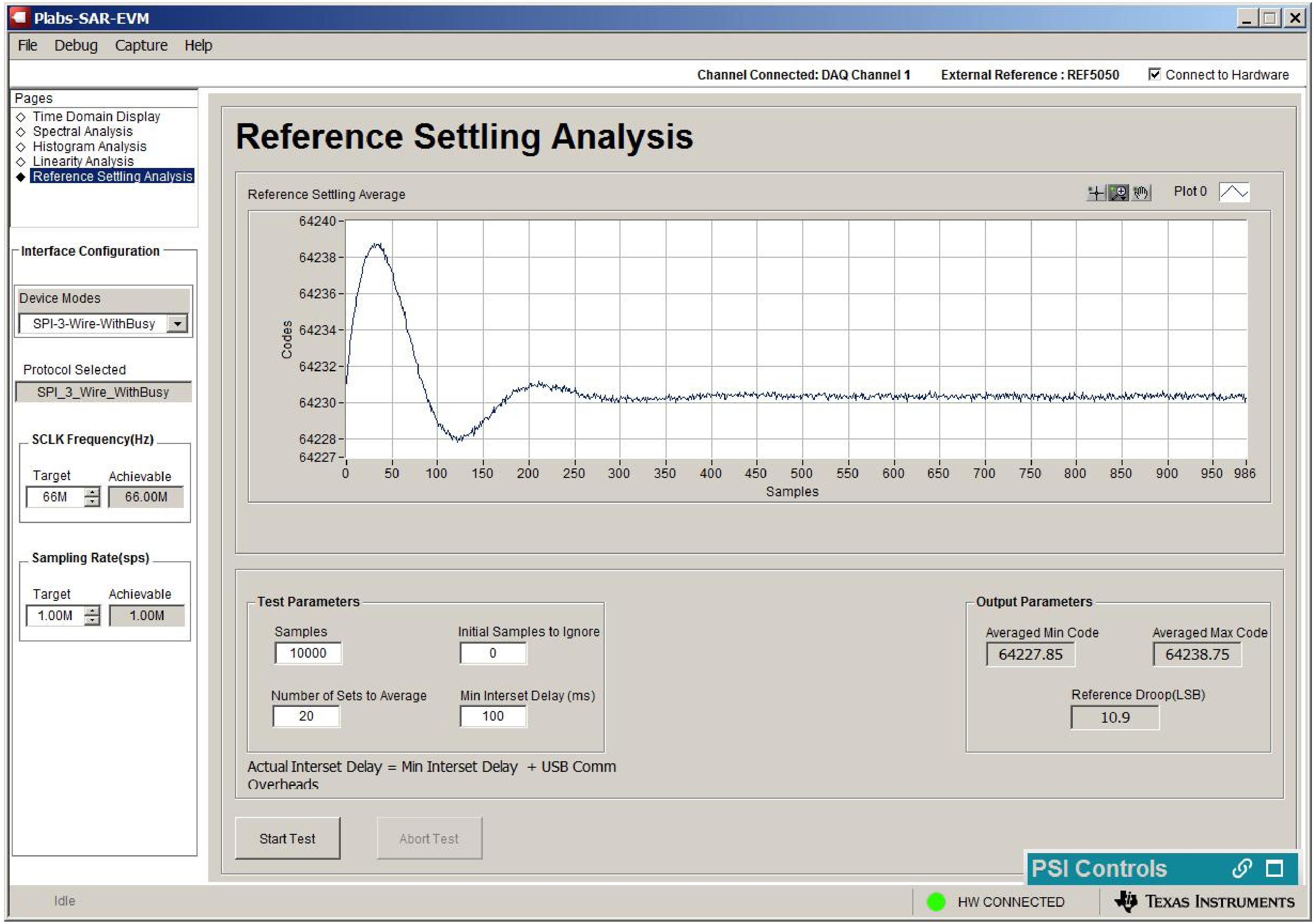
REF5050: 1Msps, Settling

	fs	Droop (LSB)
REF5050	1M	10.9



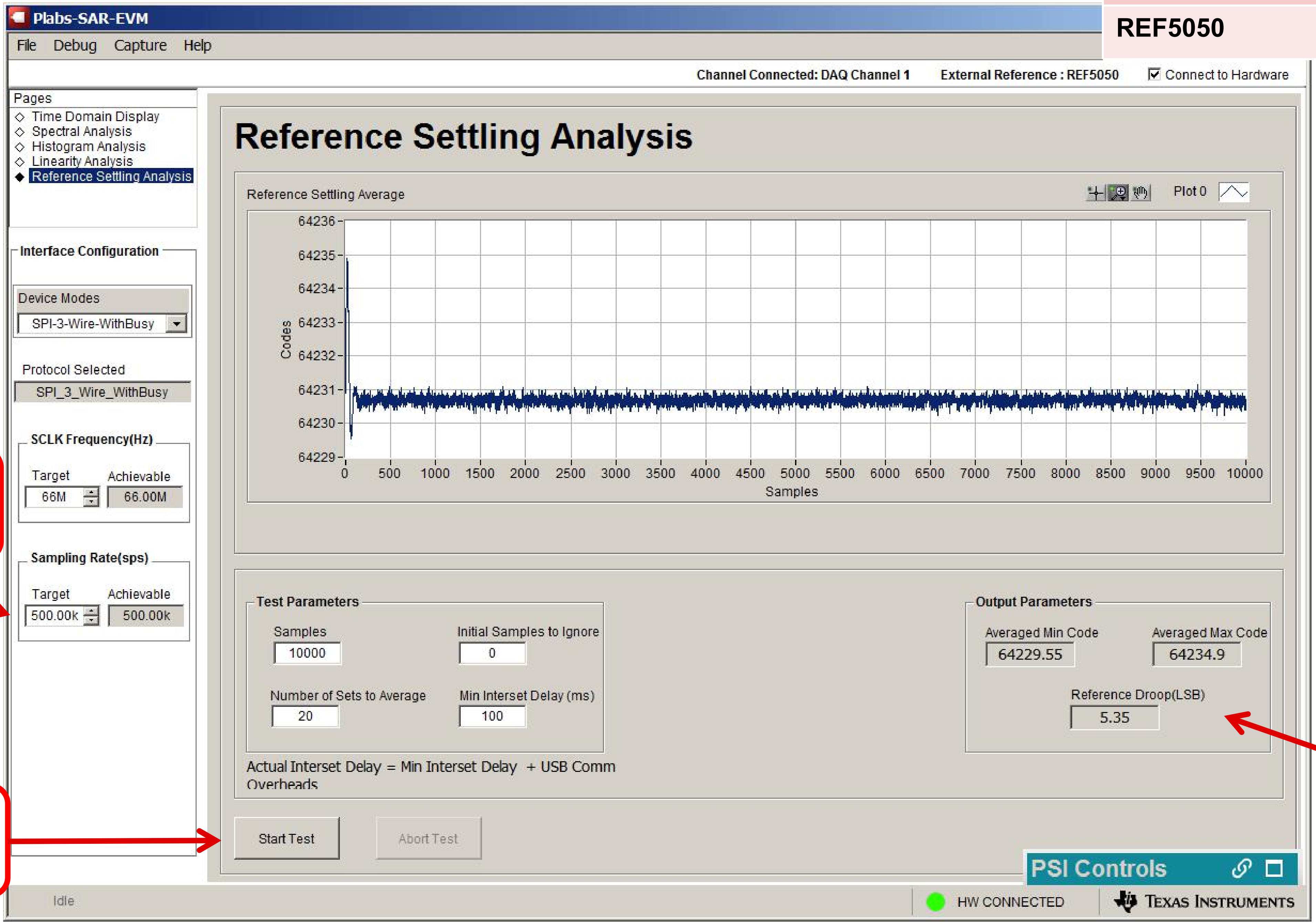
1. Sampling Rate 1Msps
2. Number of sets to average to 20.
3. Min Interset delay (ms) to 100ms.
4. Start test
5. Reference droop

Zoom in on Settling



REF5050: 500ksps, Settling

	fs	Droop (LSB)
REF5050	1M	10.9
REF5050	**500k**	**5.35**



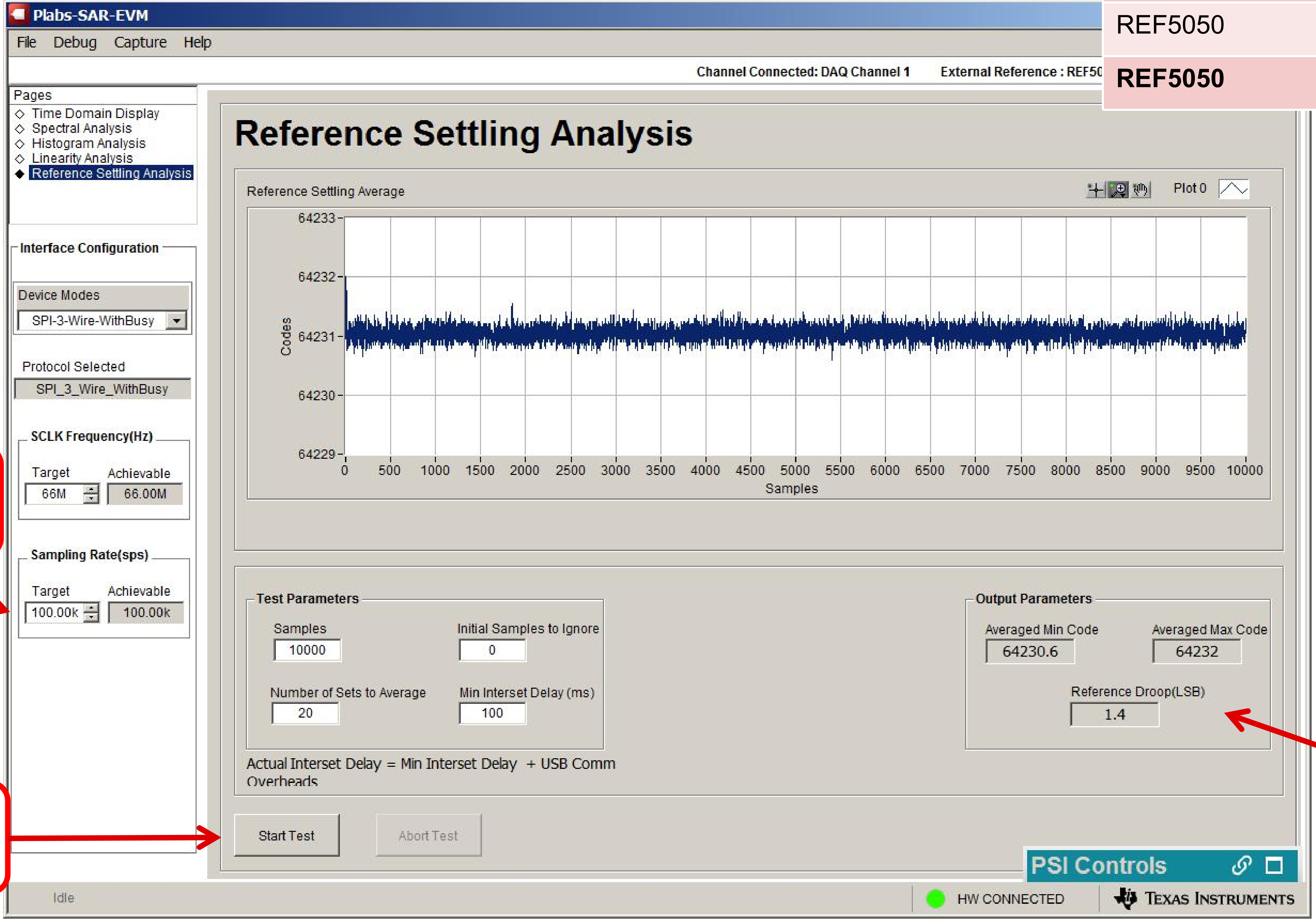
1. Sampling Rate 500ksps

2. Start test

3. Reference droop

REF5050: 100ksps, Settling

	fs	Droop (LSB)
REF5050	1M	10.9
REF5050	500k	5.35
REF5050	**100k**	**1.4**

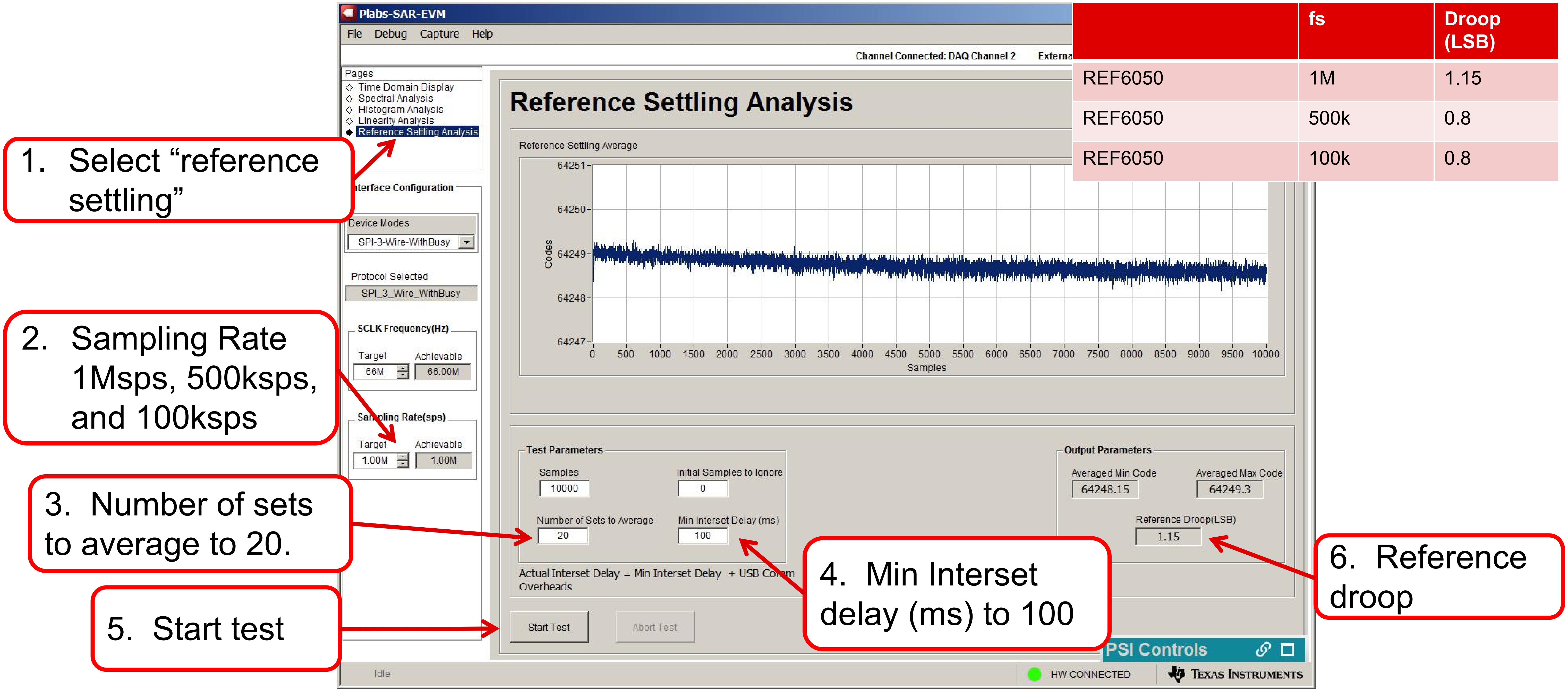


1. Sampling Rate 100ksps

2. Start test

3. Reference droop

REF6050: 1Msps, 500ksps, and 100ksps settling



	fs	Droop (LSB)
REF6050	1M	1.15
REF6050	500k	0.8
REF6050	100k	0.8

Expected results

			Example Measurements		
Reference		Sampling Rate	SNR (dB)	THD (dB)	Reference Droop Vin = 4.9V DC (codes)
	Data Sheet Typical Specification	1M	93	-108	
1	REF5050	1M	92.2	-91.4	10.9
2	REF5050	500k	92.1	-97.1	5.35
3	REF5050	100k	92.0	-108.2	1.4
4	REF6050	1M	92.6	-108.1	1.15
5	REF6050	500k	92.7	-109.3	0.8
6	REF6050	100k	92.3	-108.1	0.8

Thanks for your time!
Q & A